For full datasheet, click **HERE**.

USB Type-C / DP1.4a Alt-Mode to HDMI2.0b Protocol Converter With USB Retimer

Features

- USB Type-C DisplayPort Alt-mode de-mux
  - Simultaneous USB3.1 Gen2 and 2 lanes DP1.4a input OR 4 lanes DP1.4a input
  - Flip option for connector plug orientation
  - DP lane swap and polarity swap
- DisplayPort® (DP) ver.1.4a compliant receiver
  - Link rate 1.62 / 2.7 / 5.4 / 8.1Gbps
  - 1, 2, or 4 lanes configuration
  - AUX CH 1Mbps
  - HPD_OUT
  - Programmable receiver equalization
  - TPS4 EQ Phase LT support
  - Scrambling of main link data
  - De-spreading of link frequency
  - Video Stream Handling
    - RGB/ YCC 444/422/420 pixel format up to 16 bpc
  - DPCD and CEC
    - DPCD data structure revision 1.4
    - CEC tunneling over AUX
  - Audio stream handling
    - Non-HBR Compressed Formats
      - 2/8 ch layouts
      - Up to 192kHz sample rates
      - Dolby Digital, Digital+, Atmos
    - HBR Audio Formats
      - 8 ch layout
      - Up to 1536kHz sample rates
      - Dolby TrueHD, Atmos, DTS Master
    - LPCM Formats2/8/16/32 Ch
      - Up to 192kHz sample rates
      - 3D LPCM, speaker allocation & mapping
    - One Bit DSD Formats
      - 2/8 ch
      - Single & Double Rate
      - 12288kHz sample rates
    - DST DSD Formats
      - Single/Double rate
      - Up to 22579.2kHz
      - Audio InfoFrame/ ACM/ ISRC/ Audio Metadata DI packets
- HDMI2.0b transmitter
  - HDMI mode
    - DC-coupled output with source termination
    - 600 MHz maximum TMDS character clock
    - TMDS character-clock divide_by_4 mode
    - HPD_IN (5V Tolerant)
    - DDC CH (5V Tolerant)
    - Conversion to DVI output
  - Scrambler for HDMI output
  - Programmable signal amplitude
  - Programmable pre-emphasis control
  - Pixel format RGB / YCC 444/422/420
  - Deep color up to 16 bits per color
  - 3D video timings
  - CEC 2.0+ with snooping, tunneling
  - SCDC read request handling
  - Metadata handling
- HDMI 2.1 Features
  - Through 6GHz TMDS Mode
  - Supports 4k120Hz,4:2:0, 8bpc with Adaptive Sync to VRR conversion
  - Dynamic HDR Metadata through Extended Metadata Packet
  - Supports VRR, FVA, QMS, QFT, ALLM
- USB3.1 compliant re-timer
  - 5Gbps and 10Gbps support
  - Spread spectrum clocking
  - LFPS polling and processing
  - Lane polarity inversion
  - Bit level re-timer for SS mode
  - SRIS (Separate Reference Clock Independent SSC) for SSP mode
  - Adaptive Receiver Equalization
  - Multi-tap FIR EQ Transmitter Emphasis

Features (continued)

- Video processing
  - Color space conversion from RGB to YCC
  - Colorimetry support: BT2020, BT709, BT601, and Adobe RGB
  - Color bit depth expansion (10 to 12 bits)
  - 16 bits per color pass through
  - DP to HDMI Stereoscopic 3D Transport
    - Frame sequential to stacked top-bottom conversion
    - Pass through of other 3D formats
  - Programmable coefficient 3x3 matrix
    - Programmable input offset
    - Programmable output offset
    - Programmable output clipping levels
  - Video Horizontal blanking expansion
  - Pixel stream de-skewing
  - Adaptive Sync Video
  - Dithering
  - Chroma down sampling
    - 5-tap H & V FIR filters with programmable coefficients
    - 12 bits per color input width
    - 12 bits per color output width
    - YCbCr444 to YCbCr420 conversion
    - YCbCr444 to YCbCr422 conversion
    - YCbCr422 to YCbCr420 conversion
    - Pass through for YCbCr444/422/420
- Max video resolution and color depth on HDMI TX output
  - 4K2K60Hz, RGB/YCbCr444, 8 bpc
  - 4K2K60Hz, YCbCr420, up to 16 bpc
  - 4K2K30Hz, RGB/YCbCr444, up to 16 bpc
- HDCP support
  - HDCP1.3 to HDCP1.4 Repeater function
  - DCP compliant: HDCP2.x to HDCP1.4
  - HDCP2.x to HDCP2.x Repeater function
  - Read-protected embedded HDCP keys
- Enhanced security
  - Encrypted on-chip key storage
  - RSA-2048bit signed application firmware
  - Secure boot
  - Secure In-System-Programming
  - Test, debug ports deactivation
- Metadata handling
  - HDMI TX DVI/HDMI mode setting (DPCD register)
  - YCbCr444-420 conversion (DPCD register)
  - IEC60958 BYTE3 channel status overwrite
  - CTA861G INFO FRAME generation
  - CTA861.3 HDR and Mastering InfoFrame
  - Chainable VSC_EXT SDP packing format
- ARM processor and peripheral controllers
  - ARM Cortex M3 core
  - SPI controller
  - I2C master, slave controller
  - On-Chip, RAM, ROM, OTP
- Device configuration options
  - Application FW stored in SPI flash
  - AUX CH, I2C host interface
- Internal video pattern generator
  - Configurable through vendor specific DPCD registers
- EMI reduction support
  - Spread spectrum for DP input, output
  - Scrambler for DP and HDMI outputs
- Low power operation
  - 900mW nominal operation with retimer
  - 650mW nominal operation without retimer
  - 9.2mW Standby operation
- ESD specification
  - ESD: ±2kV HBM, 250V CDM
- Package
  - TFBGA-169, 7.0mm x 7.0mm x 1.2mm
  - Halogen free RoHS and Green Compliant
- Power supply voltages
  - 1.8V I/O, 0.95V core

Description

The MCDP5200 is an advanced USB Type-C / DisplayPort1.4a to HDMI2.0b protocol converter with an integrated USB type-C de-multiplexer, targeted primarily for Mobile Notebook accessory and display applications. This device functions as a DP to HDMI protocol converter with an HDCP1.x/ HDCP2.x repeater function.

The MCDP5200 has a DP alt-mode capable USB Type-C Upstream Facing Port (UFP). The four high speed lanes of UFP can receive DP1.4a audio-video and USB3.1 Gen2 data streams simultaneously. The input lane mapping is flexible and meets the USB Type-C connector flip orientation requirements. The incoming DP and USB signals are de-multiplexed, retimed, and transmitted on the Downstream Facing Ports (DFP). The MCDP5200 consists of a USB DFP port with USB3.1 TX and RX pair and an audio-video DFP port configured as DC coupled HDMI/DVI port, each with four high-speed lanes.

The combo receiver in MCDP5200 supports all DP standard data rates up to HBR3 (8.1Gbps/lane) and USB3.1 Gen1 (5.0Gbps) and Gen2 (10.0Gbps). The transmitter supports TMDS data format up to 6.0Gbps/lane. The side-band channel uses 1.0 Mbps Manchester-coded AUX signaling for DP and DDC signaling up to 100 kbps for the HDMI interface.

In the protocol converter mode, MCDP5200 translates a DP SST stream into DC coupled HDMI2.0b output. The highest video timing supported in this mode is 4k2k60Hz RGB/YCC 444 or 4k2k120Hz in YCC 420-pixel format. It supports both RGB 444 and YCC444/422/420 video pixel encoding formats with a color depth up to 16 bpc (bits per component or 48 bits per pixel). The MCDP5200 also has a pixel processing unit capable of video color space conversion from RGB444 to YCC444 with bit depth expansion and pixel encoding format conversion from YCC444 to YCC422/420. It also supports advanced dithering function to truncate the pixel bit depth to the precision of the connected sink device. Pixel format conversion along with horizontal blanking expansion improves interoperability and smooth rendering of video from mobile PC and tablets on legacy TVs. Besides, MCDP5200 also supports HDMI CEC tunneling over DP AUX channel for remote control pass-through, one touch control of the connected devices in a CE system.

The MCDP5200 processes High Dynamic Range (HDR) video content specified in BT601, BT709, BT2020 or in the Adobe RGB colorimetry format with the appropriate metadata conversion from DP to HDMI standard. It also offers secure reception and transmission of high bandwidth digital audio and video content with HDCP1.x or HDCP2.x content protection. MCDP5200 functions as an HDCP1.x and HDCP2.x repeater between the DP source and DP or HDMI sink.

The MCDP5200 uses an external crystal of 25MHz as a reference clock for its operation. It has a 300MHz ARM Cortex M3 CPU with on-chip memories for storing data and code execution. The peripheral subsystem includes SPI, UART (debug only), and I2C master and slave interfaces. An internal Power-On Reset (POR) circuit senses the voltage on the reset input and provides the chip reset during system power-up. The MCDP5200 uses an external 16Mbit SPI flash memory for storing the RSA-2048 signed application firmware with fail-safe recovery. At boot up, the CPU goes through a secure boot process authenticating the application code image stored in the SPI flash. It supports both standard mode and quad mode operation. A firmware update of the SPI flash is done securely through the DP AUX_CH or I2C host interface (Secure In-System-Programming).

Applications Information

The target applications of MCDP5200 are the notebook, tablet accessories i.e., adapters (dongles), docking stations and other AV accessories. It is also intended for enabling USB Type-C DP alternative mode for inside-the-box applications such as TVs, signage game consoles and other consumer equipment.

Adapter (Dongle) Application

In a dongle topology the MCDP5200 is part of the source side adaptor that plugs into a DP source device via a USB Type-C or a DisplayPort connector at the upstream facing port. In a typical DP-to-HDMI dongle application, MCDP5200 functions as a system master and operates as a protocol converter. In a USB type-C to HDMI dongle it can also function as a Type-C Port Manager (TCPM) along with an external TCPC device (e.g. Kinetic MCDP9000 TCPC). The upstream source typically powers the dongle.

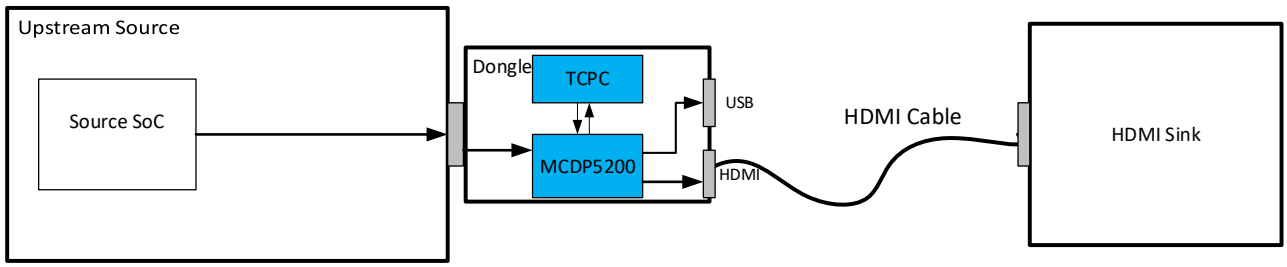

Figure 1. MCDP5200 Adapter Use Case

Docking Station Application

In a docking station topology, the MCDP5200 is part of a larger system which connects to a DP source device via a custom connector or USB-Type-C Alt-Mode receptacle on the upstream facing port. In a docking station design the MCDP5200 typically co-exists with other system components such as the system host, MST hub, and USB hub. In this application, the MCDP5200 functions as a protocol converter and HDCP repeater.

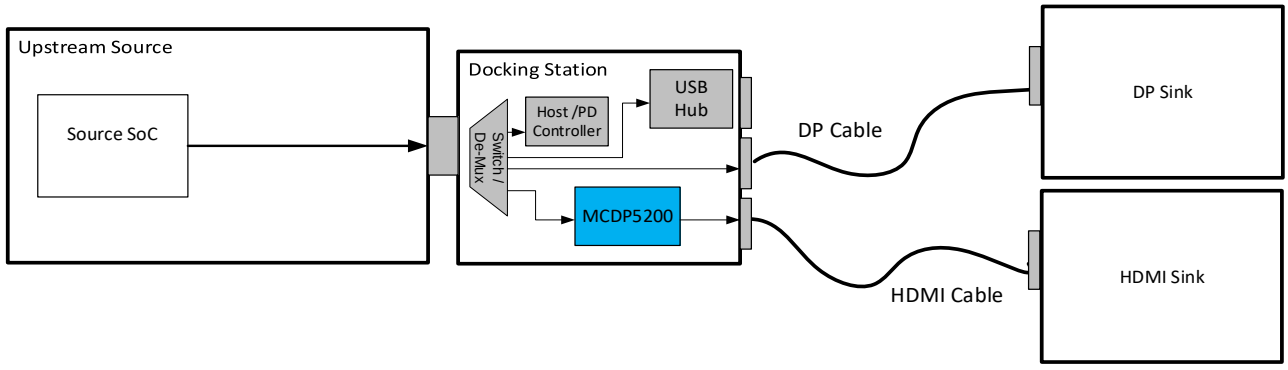

Figure 2. MCDP5200 Docking Station Use Case

TV, Digital Signage Application

TV or a signage system featuring the USB Type-C connector supporting the DP Alt-mode requires a DP-to-HDMI protocol converter. The MCDP5200 is an ideal fit for such applications; it supports video resolution up to 4K60Hz over 2 lanes with HDR video quality for deep color media playback, end-to-end HDCP2.x content protection, and CEC tunneling over DP AUX CH for single-point remote-control access for all connected devices.

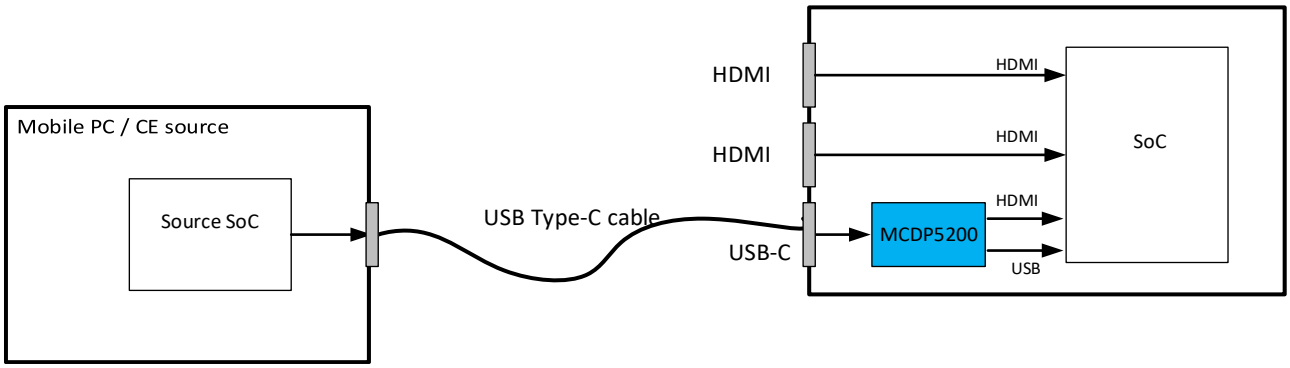

Figure 3. MCDP5200 TV, Digital Signage Use Case

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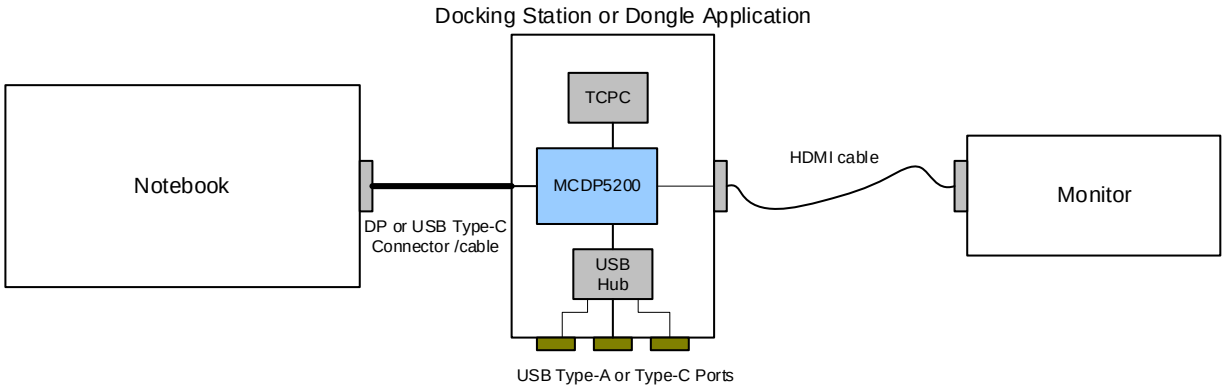
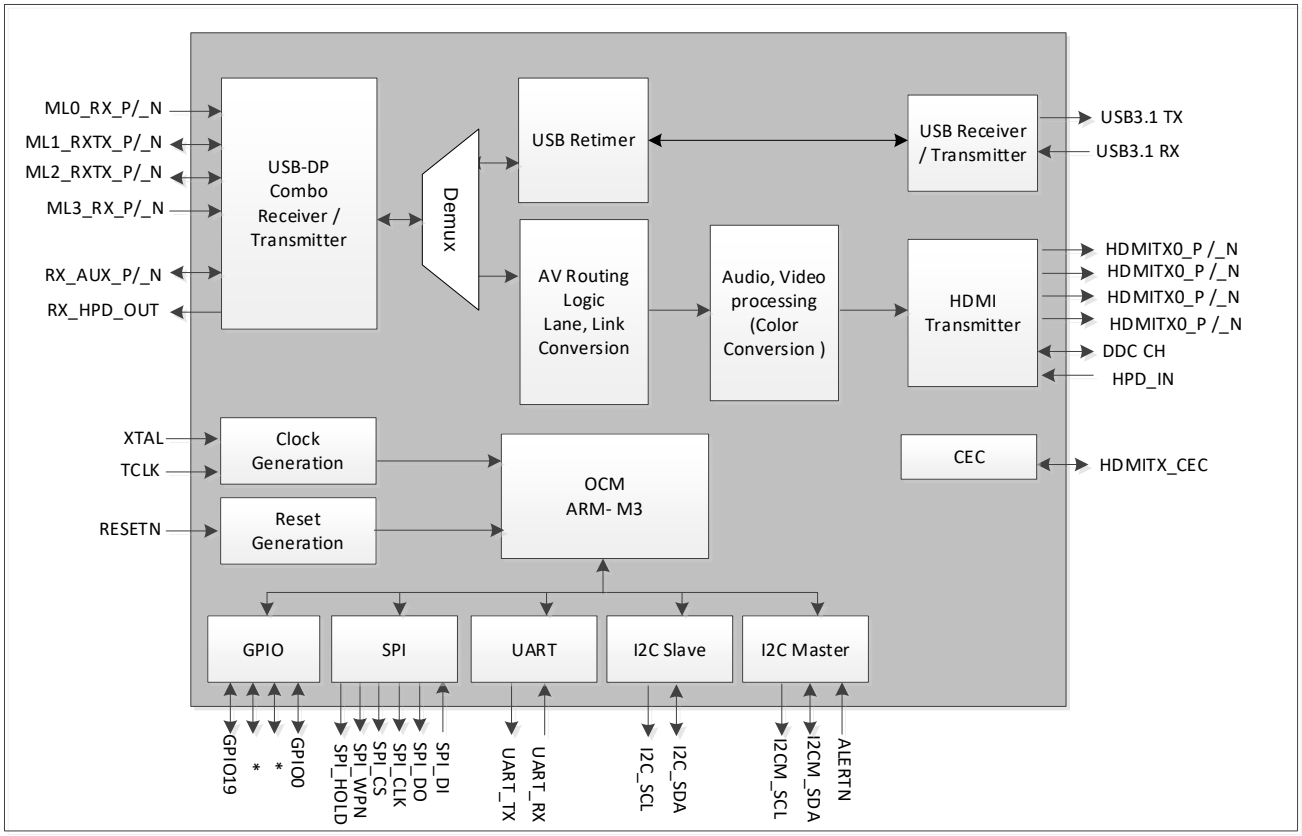
Typical Simplified Application Diagram



Functional Block Diagram



Ordering Information

Part Number	Functional Description	Marking[1]	Operating Temperature	Package	External Package
MCDP5200B0	USB-C to HDMI2.0/USB-A (with USB retimer)	YYWWxxxx	0°C to +70°C	TFBGA-169	TRAYS
MCDP5200B0T					Tape and Reel

1. “YYWWxxxx” is the date code, assembly code and lot number.