Microsemi Corporation
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Customer Notification No: CN1674

Customer Advisory Notice (CAN)

Subject: Resetting SmartFusion Device After In-Application Programming (IAP) Under Certain Conditions

Description

During IAP programming, if an external clock source is used to drive the phase-locked loop (PLL) that is used to clock the microcontroller subsystem (MSS), a SmartFusion® device may hang at the end of the IAP operation. Any SmartFusion device could potentially have this problem. The list of SmartFusion part numbers is provided in Appendix A.

When switching between programming and operational modes, in-rush current causes the PLL to lose the lock signal as well as the clock. In some instances the clock never recovers. Since the ARM Cortex-M3 in the SmartFusion device depends on the clock source for proper operation, it no longer can function in this scenario. This behavior does not occur in standard programming or when the internal oscillator is used to drive the MSS clock.

Workaround

To mitigate this issue, a software workaround has been identified which involves performing a system reset at the end of the IAP operation, instead of the normal ISC_DISABLE instruction. This resets the device and the Cortex-M3. This workaround will be available with the MSS IAP driver v2.3 by 11th November, 2016. This IAP software version will be available through the Firmware Catalog.

This IAP software release has a variable called **enable_system_reset_on_exit** defined in the **dp_user.c** file. The default value of this variable is TRUE to perform the reset operation at the end of the IAP operation. You may choose to set it to FALSE if you want the device to go through the normal process of exiting programming mode, avoiding the system reset. Manual setting may be desired if the internal oscillator is used to drive the MSS clock as the device hang behavior is not observed in this use model.

Till the time updated IAP software is available, you can change the code manually by calling NVIC_SystemReset ( ) function in the dp_exit ( ) function as shown in the following code snippet:

```
    void dp_exit(void)
    {
#ifdef NVM_SUPPORT
if (
((device_family & SFS_BIT) == SFS_BIT) &&
(dat_support_status | (NVM0_DAT_SUPPORT_BIT | NVM1_DAT_SUPPORT_BIT |
NVM2_DAT_SUPPORT_BIT | NVM3_DAT_SUPPORT_BIT)) &&
(
(Action_code == DP_PROGRAM_ACTION_CODE) ||
(Action_code == DP_VERIFY_ACTION_CODE) ||
(Action_code == DP_PROGRAM_NVM_ACTION_CODE) ||
```

```
(Action_code == DP_VERIFY_NVM_ACTION_CODE) ||
(Action_code == DP_PROGRAM_PRIVATE_CLIENTS_ACTION_CODE) ||
(Action_code == DP_VERIFY_PRIVATE_CLIENTS_ACTION_CODE) ||
(
((device_family & SFS_BIT) == SFS_BIT) &&
((Action_code   ==   DP_PROGRAM_ARRAY_ACTION_CODE)   ||(Action_code   ==
DP_VERIFY_ARRAY_ACTION_CODE))
)
)
)
{
      dp_exit_access_nvm();
}
#endif
      NVIC_SystemReset();
       while( 1 )
         {
                 ;
            }
     return;
}
```

Note: Before compiling the code, add the below header file in the `dpalg.c file`:
 `#include "a2fxxxm3.h"`

Appendix A: SmartFusion Device List

A2F060	A2F200	A2F500
A2F060M3E-1CS288	A2F200M3F-1CS288	A2F500M3G-1CS288
A2F060M3E-1CS288I	A2F200M3F-1CS288I	A2F500M3G-1CS288I
A2F060M3E-1CSG288	A2F200M3F-1CSG288	A2F500M3G-1CSG288
A2F060M3E-1CSG288I	A2F200M3F-1CSG288I	A2F500M3G-1CSG288I
A2F060M3E-1FG256	A2F200M3F-1FG256	A2F500M3G-1FG256
A2F060M3E-1FG256I	A2F200M3F-1FG256I	A2F500M3G-1FG256I
A2F060M3E-1FG256M	A2F200M3F-1FG484	A2F500M3G-1FG256M
A2F060M3E-1FGG256	A2F200M3F-1FG484I	A2F500M3G-1FG484
A2F060M3E-1FGG256I	A2F200M3F-1FGG256	A2F500M3G-1FG484I
A2F060M3E-1FGG256M	A2F200M3F-1FGG256I	A2F500M3G-1FG484M
A2F060M3E-1TQ144	A2F200M3F-1FGG484	A2F500M3G-1FGG256
A2F060M3E-1TQ144I	A2F200M3F-1FGG484I	A2F500M3G-1FGG256I
A2F060M3E-1TQG144	A2F200M3F-1PQ208	A2F500M3G-1FGG256M
A2F060M3E-1TQG144I	A2F200M3F-1PQ208I	A2F500M3G-1FGG484
A2F060M3E-CS288	A2F200M3F-1PQG208	A2F500M3G-1FGG484I
A2F060M3E-CS288I	A2F200M3F-1PQG208I	A2F500M3G-1FGG484M
A2F060M3E-CSG288	A2F200M3F-CS288	A2F500M3G-1PQ208
A2F060M3E-CSG288I	A2F200M3F-CS288I	A2F500M3G-1PQ208I
A2F060M3E-FG256	A2F200M3F-CSG288	A2F500M3G-1PQG208
A2F060M3E-FG256I	A2F200M3F-CSG288I	A2F500M3G-1PQG208I
A2F060M3E-FG256M	A2F200M3F-FG256	A2F500M3G-CS288
A2F060M3E-FGG256	A2F200M3F-FG256I	A2F500M3G-CS288I
A2F060M3E-FGG256I	A2F200M3F-FG484	A2F500M3G-CSG288
A2F060M3E-FGG256M	A2F200M3F-FG484I	A2F500M3G-CSG288I
A2F060M3E-TQ144	A2F200M3F-FGG256	A2F500M3G-FG256
A2F060M3E-TQ144I	A2F200M3F-FGG256I	A2F500M3G-FG256I
A2F060M3E-TQG144	A2F200M3F-FGG484	A2F500M3G-FG256M
A2F060M3E-TQG144I	A2F200M3F-FGG484I	A2F500M3G-FG484
-	A2F200M3F-PQ208	A2F500M3G-FG484I
-	A2F200M3F-PQ208I	A2F500M3G-FG484M
-	A2F200M3F-PQG208	A2F500M3G-FGG256
-	A2F200M3F-PQG208I	A2F500M3G-FGG256I
-	-	A2F500M3G-FGG256M
-	-	A2F500M3G-FGG484
-	-	A2F500M3G-FGG484I
-	-	A2F500M3G-FGG484M
-	-	A2F500M3G-PQ208
-	-	A2F500M3G-PQ208I
-	-	A2F500M3G-PQG208
-	-	A2F500M3G-PQG208I

Contact Information

If you have any questions, please contact Microsemi's SoC technical support at soc_tech@microsemi.com.

Regards,

Microsemi Corporation

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