PBSS5350SS

50 V, 2.7 A PNP/PNP low V_{CEsat} (BISS) transistor

Rev. 01 — 3 April 2007 **Product data sheet**

1. Product profile

1.1 General description

PNP/PNP double low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a medium power Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number	Package		NPN/PNP complement	NPN/NPN complement
	NXP	**Name**		
PBSS5350SS	SOT96-1	SO8	PBSS4350SPN	PBSS4350SS

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Dual low power switches (e.g. motors, fans)
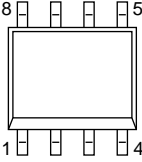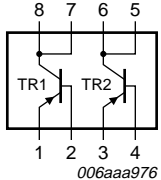- Automotive

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	−50	V
I_C	collector current		-	-	−2.7	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	−5	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -2$ A; $I_B = -200$ mA	[1] -	95	140	mΩ

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.

2. Pinning information

Table 3.   Pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR1		
3	emitter TR2		
4	base TR2		
5	collector TR2		
6	collector TR2		
7	collector TR1		
8	collector TR1		

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3. Ordering information

Table 4.   Ordering information

Type number	Package		
	Name	Description	Version
PBSS5350SS	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5.   Marking codes

Type number	Marking code
PBSS5350SS	5350SS

5. Limiting values

Table 6.   Limiting values
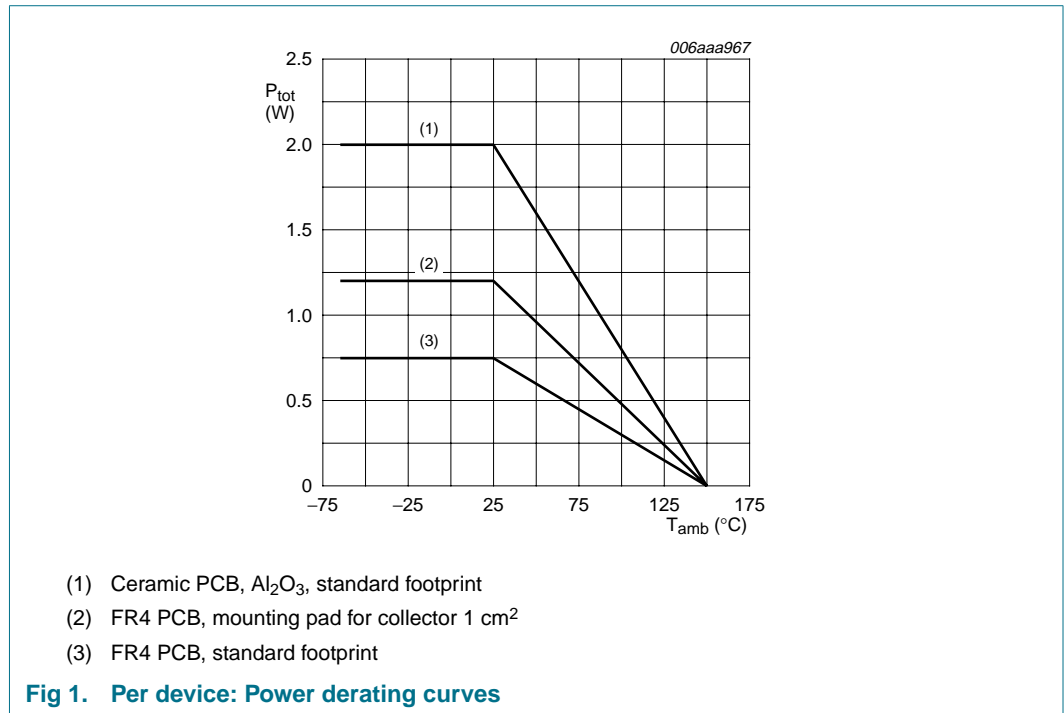*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	−50	V
V_{CEO}	collector-emitter voltage	open base		-	−50	V
V_{EBO}	emitter-base voltage	open collector		-	−5	V
I_C	collector current			-	−2.7	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	−5	A
I_B	base current			-	−0.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	0.55	W
			[2]	-	0.87	W
			[3]	-	1.43	W

Table 6.   Limiting values …*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per device						
P$_{tot}$	total power dissipation	T$_{amb}$ ≤ 25 °C	[1]	-	0.75	W
			[2]	-	1.2	W
			[3]	-	2	W
T$_j$	junction temperature			-	150	°C
T$_{amb}$	ambient temperature			−65	+150	°C
T$_{stg}$	storage temperature			−65	+150	°C

[1]   Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2]   Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

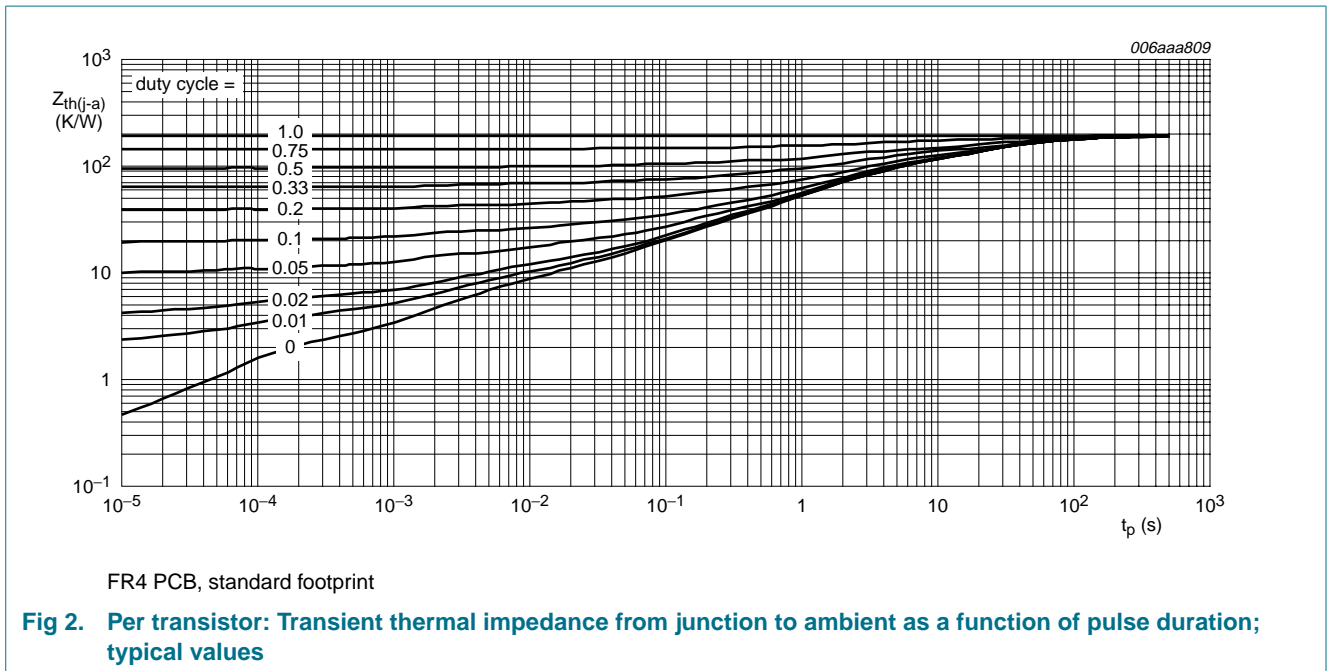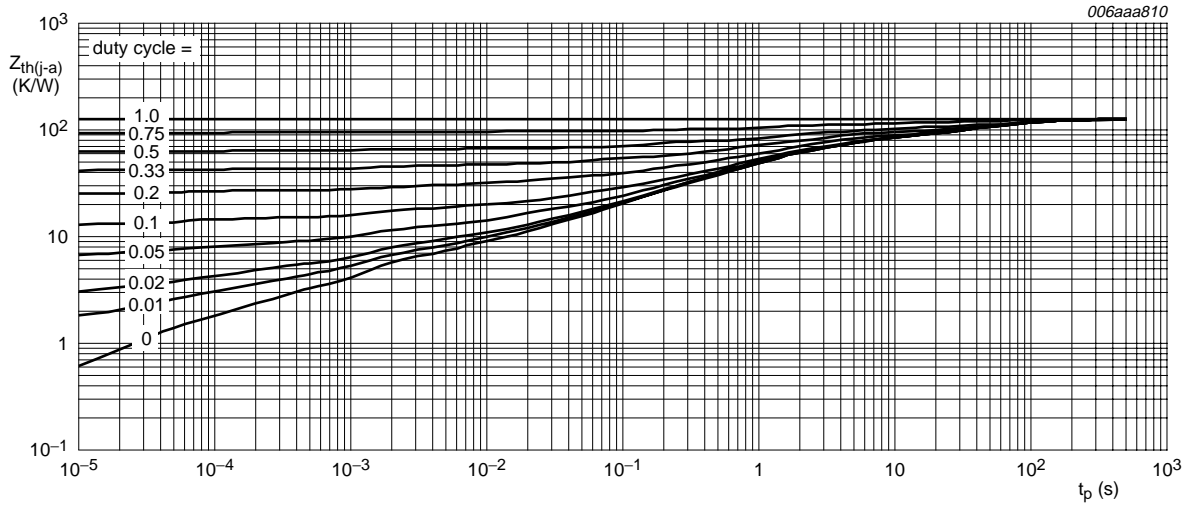[3]   Device mounted on a ceramic PCB, Al$_2$O$_3$, standard footprint.

(1)   Ceramic PCB, Al$_2$O$_3$, standard footprint

(2)   FR4 PCB, mounting pad for collector 1 cm^2

(3)   FR4 PCB, standard footprint

Fig 1.   Per device: Power derating curves

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6. Thermal characteristics

Table 7.   Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R$_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	227	K/W
			[2]	-	-	144	K/W
			[3]	-	-	87	K/W
R$_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	40	K/W
Per device							
R$_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	167	K/W
			[2]	-	-	104	K/W
			[3]	-	-	63	K/W

[1]   Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2]   Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3]   Device mounted on a ceramic PCB, Al$_2$O$_3$, standard footprint.

FR4 PCB, standard footprint

Fig 2.   Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

FR4 PCB, mounting pad for collector 1 cm^2

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values
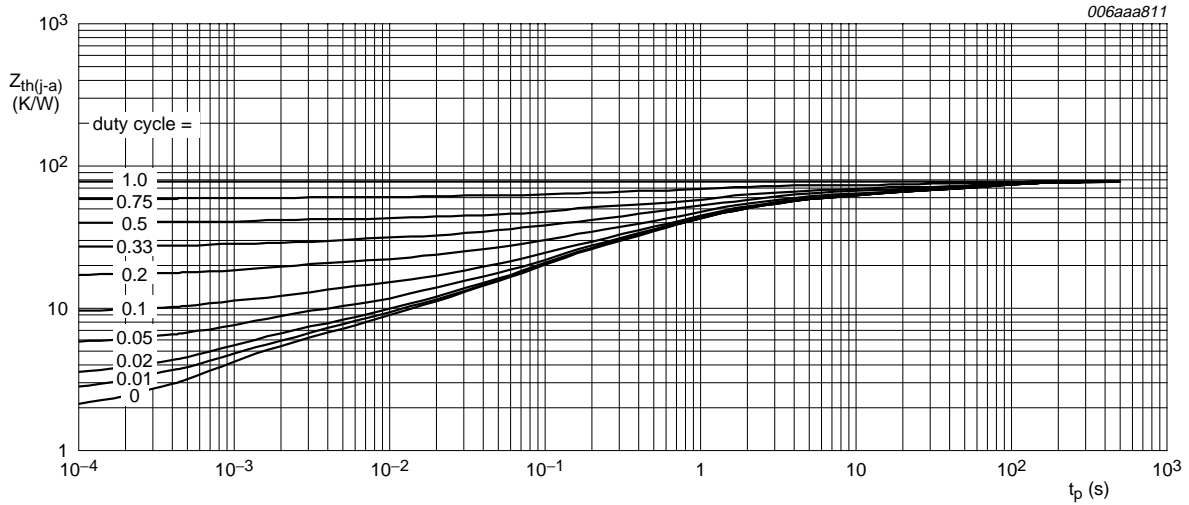
Ceramic PCB, Al$_2$O$_3$, standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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7. Characteristics

Table 8. Characteristics

$T_{amb} = 25\,°C$ unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
I_{CBO}	collector-base cut-off current	$V_{CB} = -50$ V; $I_E = 0$ A		-	-	−100	nA
		$V_{CB} = -50$ V; $I_E = 0$ A; $T_j = 150\,°C$		-	-	−50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -50$ V; $V_{BE} = 0$ V		-	-	−100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5$ V; $I_C = 0$ A		-	-	−100	nA
h_{FE}	DC current gain	$V_{CE} = -2$ V; $I_C = -100$ mA		200	340	-	
		$V_{CE} = -2$ V; $I_C = -500$ mA	[1]	200	290	-	
		$V_{CE} = -2$ V; $I_C = -1$ A	[1]	180	250	-	
		$V_{CE} = -2$ V; $I_C = -2$ A	[1]	130	180	-	
		$V_{CE} = -2$ V; $I_C = -2.7$ A	[1]	95	135	-	
V_{CEsat}	collector-emitter saturation voltage		[1]				
		$I_C = -0.5$ A; $I_B = -50$ mA		-	−60	−90	mV
		$I_C = -1$ A; $I_B = -50$ mA		-	−125	−180	mV
		$I_C = -2$ A; $I_B = -100$ mA		-	−225	−320	mV
		$I_C = -2$ A; $I_B = -200$ mA		-	−190	−280	mV
		$I_C = -2.7$ A; $I_B = -270$ mA		-	−255	−370	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = -2$ A; $I_B = -200$ mA	[1]	-	95	140	mΩ
V_{BEsat}	base-emitter saturation voltage		[1]				
		$I_C = -2$ A; $I_B = -100$ mA		-	−0.95	−1.1	V
		$I_C = -2.7$ A; $I_B = -270$ mA		-	−1	−1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2$ V; $I_C = -1$ A	[1]	-	−0.8	−1.2	V
t_d	delay time	$V_{CC} = -10$ V; $I_C = -2$ A; $I_{Bon} = -100$ mA; $I_{Boff} = 100$ mA		-	9	-	ns
t_r	rise time			-	54	-	ns
t_{on}	turn-on time			-	63	-	ns
t_s	storage time			-	190	-	ns
t_f	fall time			-	50	-	ns
t_{off}	turn-off time			-	240	-	ns
C_c	collector capacitance	$V_{CB} = -10$ V; $I_E = i_e = 0$ A; $f = 1$ MHz		-	25	35	pF

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.
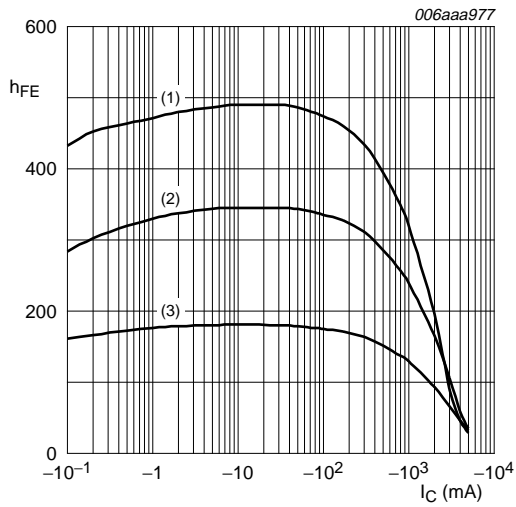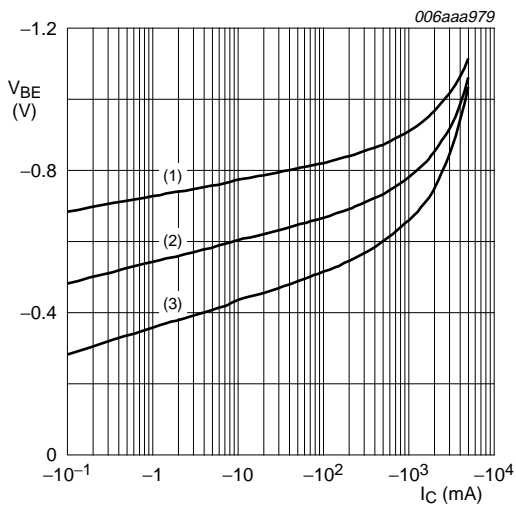
$V_{CE} = -2$ V

(1) T$_{amb}$ = 100 °C

(2) T$_{amb}$ = 25 °C

(3) T$_{amb}$ = −55 °C

Fig 5. DC current gain as a function of collector current; typical values
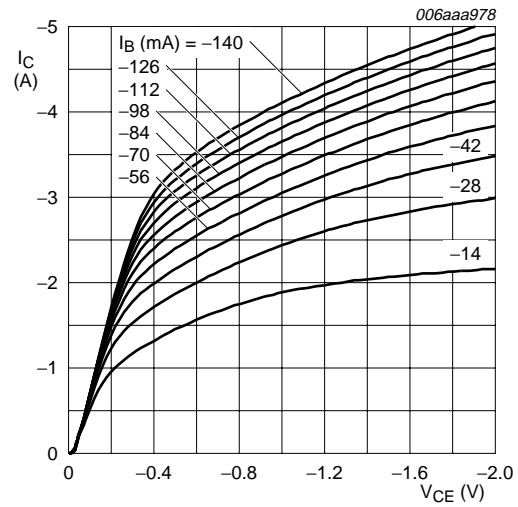
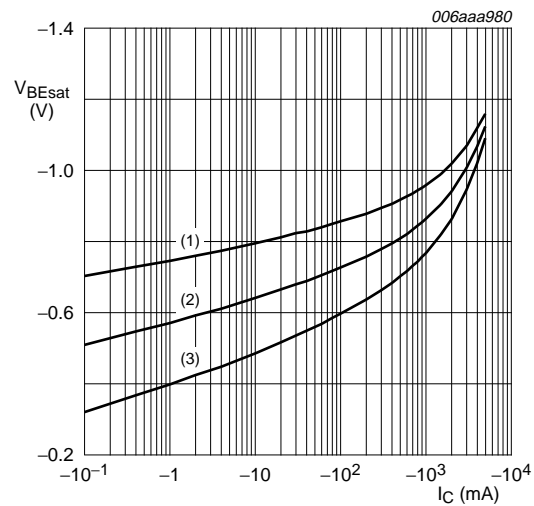T$_{amb}$ = 25 °C

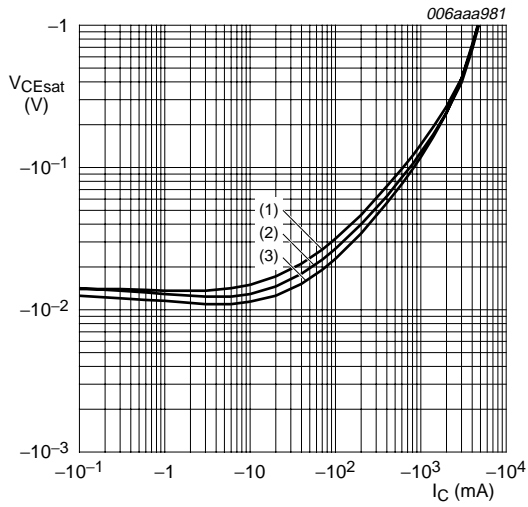**Fig 6. Collector current as a function of collector-emitter voltage; typical values**

$V_{CE} = -2$ V

(1) T$_{amb}$ = −55 °C

(2) T$_{amb}$ = 25 °C

(3) T$_{amb}$ = 100 °C

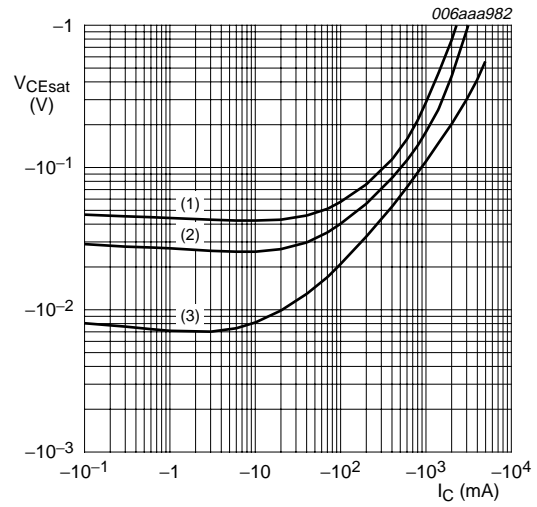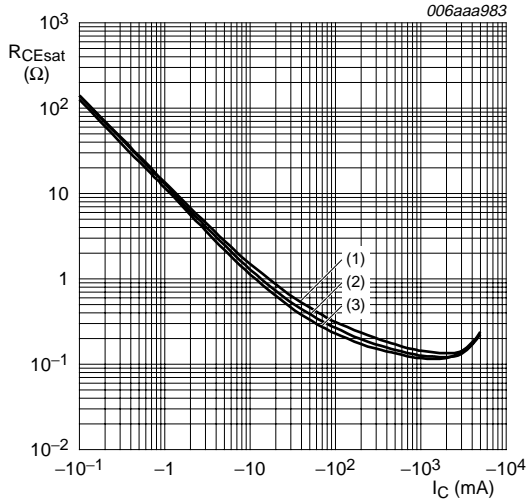**Fig 7. Base-emitter voltage as a function of collector current; typical values**

$I_C/I_B = 20$

(1) T$_{amb}$ = −55 °C

(2) T$_{amb}$ = 25 °C

(3) T$_{amb}$ = 100 °C

Fig 8. Base-emitter saturation voltage as a function of collector current; typical values

I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values
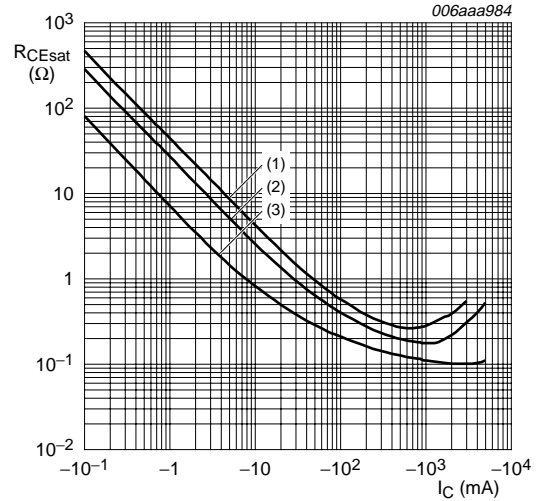

T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values

I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

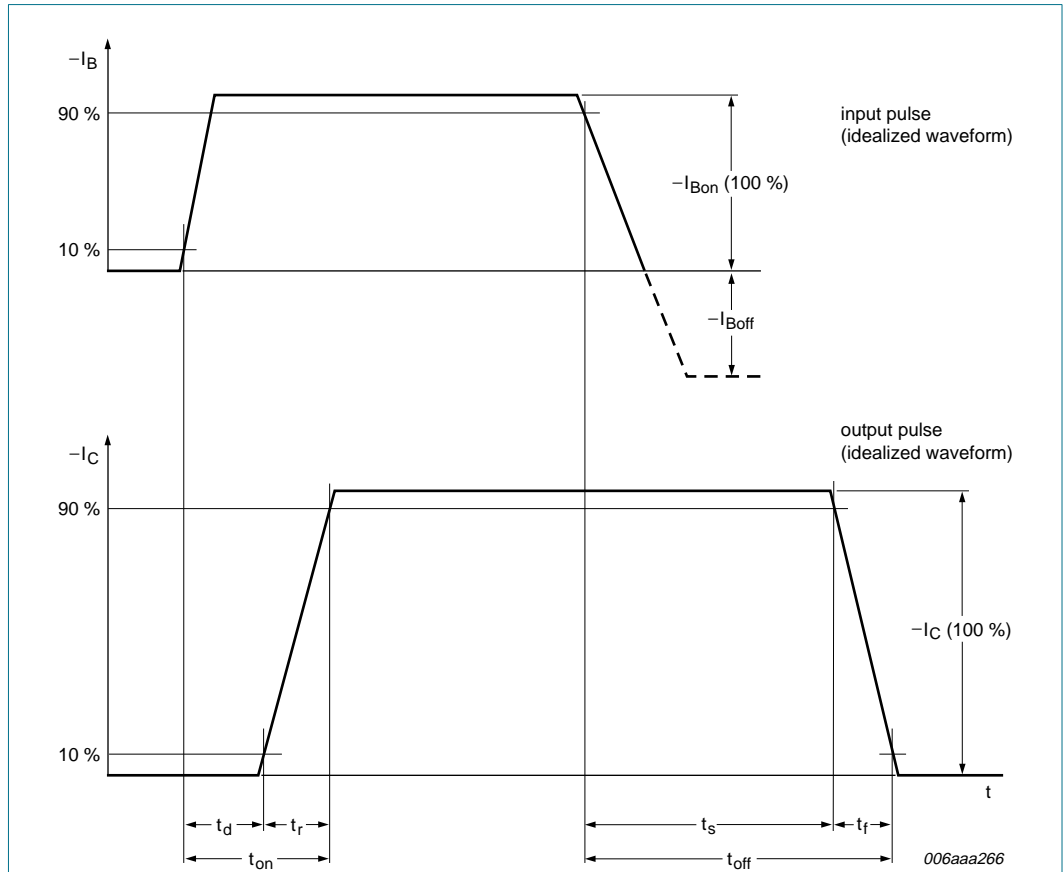**Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values**

T_{amb} = 25 °C

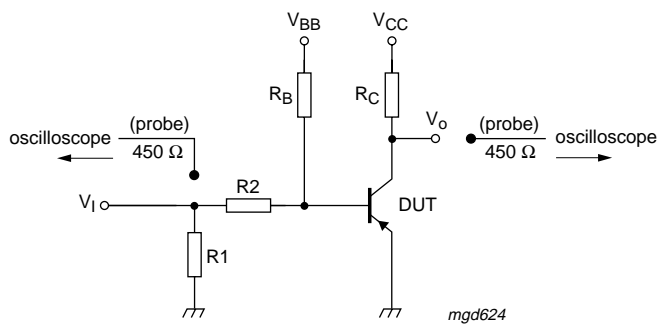(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values
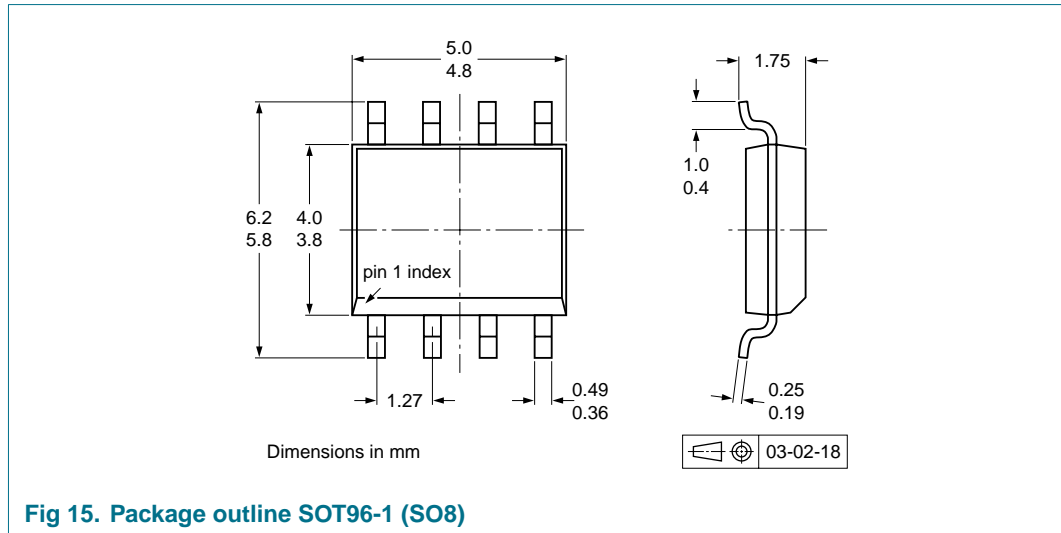
8. Test information

Fig 13. BISS transistor switching time definition

$V_{CC} = -10$ V; $I_C = -2$ A; $I_{Bon} = -100$ mA; $I_{Boff} = 100$ mA

Fig 14. Test circuit for switching times

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50 V, 2.7 A PNP/PNP low V_{CEsat} (BISS) transistor

9. Package outline

Fig 15. Package outline SOT96-1 (SO8)
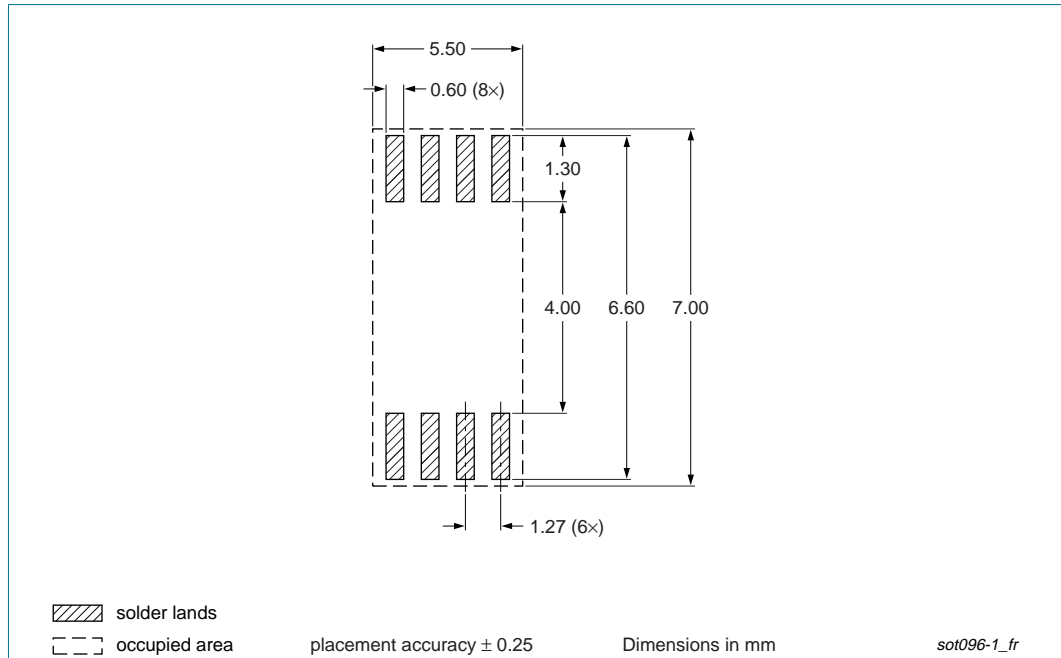
10. Packing information

Table 9. Packing methods
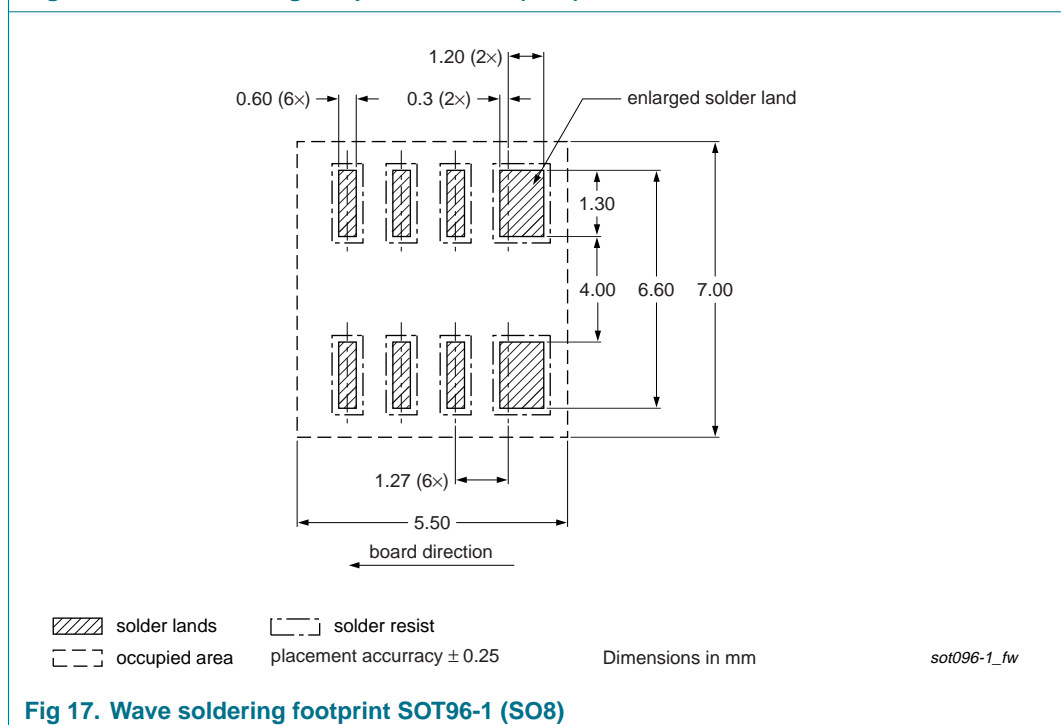*The indicated -xxx are the last three digits of the 12NC ordering code.*[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PBSS5350SS	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see Section 14.

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11. Soldering

solder lands
occupied area   placement accuracy ± 0.25   Dimensions in mm   *sot096-1_fr*

Fig 16. Reflow soldering footprint SOT96-1 (SO8)

solder lands   solder resist
occupied area   placement accurracy ± 0.25   Dimensions in mm   *sot096-1_fw*

Fig 17. Wave soldering footprint SOT96-1 (SO8)

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12. Revision history

Table 10.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5350SS_1	20070403	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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