Data Sheet, DS 1, Nov. 2001

T-SMINTO
4B3T Second Gen. Modular ISDN NT (Ordinary)

PEF 80902 Version 1.1

Wired Communications

Infineon technologies

Never stop thinking.

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Revision History: **2001-11-12** DS 1

Previous Version: Preliminary Data Sheet 06.01

Page	Subjects (major changes since last revision)
Table 10 **Figure 12** **Chapter 2.3.7.4**	Additional C/I-command LTD
Chapter 4.2	Input Leakage Current AIN, BIN: max. 30µA
Chapter 4.4	Reduced power consumption

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1 Overview

The **PEB 80902** (T-SMINT®O) offers all NT1 features known from the PEB 8090 [9] and can hence replace the latter in all NT1 applications.

Table 1 on **Page 1** summarizes the 2nd generation NT products.

Table 1 NT Products of the 2nd Generation

	PEF 80902	**PEF 81902**	**PEF 82902**
	T-SMINT®O	**T-SMINT®IX**	**T-SMINT®I**
Package	P-MQFP-44	P-MQFP-64 P-TQFP-64	P-MQFP-64 P-TQFP-64
Register access	no	U+S+HDLC+ IOM®–2	U+S+IOM®–2
Access via	n.a	parallel (or SCI or IOM®–2)	parallel (or SCI or IOM®–2)
MCLK, watchdog timer, SDS, BCL, D-channel arbitration, IOM®–2 access and manipulation etc. provided	no	yes	yes
HDLC controller	no	yes	no
NT1 mode available	yes (only)	no	no

1.1 References

[1] TS 102 080, Transmission and Multiplexing; ISDN basic rate access; Digital transmission system on metallic local lines, ETSI, November 1998

[2] FTZ 1 TR 220 Technische Richtlinie, Spezifikation der ISDN Schnittstelle Uk0 Schicht 1, Deutsche Telecom AG, August 1991

[3] TS 0284/96 Technische Spezifikation Intelligenter Netzabschluß (iNT) mit den Funktionen eines Terminaladapters TA 2a/b (ohne Internverkehr), Deutsche Telekom AG, März 2001

[4] pr ETS 300 012 Draft, ISDN; Basic User Network Interface (UNI), ETSI, November 1996

[5] T1.605-1991, ISDN-Basic Access Interface for S and T Reference Points (Layer 1 Specification), ANSI, 1991

[6] I.430, ISDN User-Network Interfaces: Layer 1 Recommendations, ITU, November 1988

[7] IEC-T, ISDN Echocancellation Circuit, PEB 20901 (IEC - TD) / PEB 20902 (IEC - TA), preliminary Target Specification 11.88, Siemens AG, 1988

[8] SBCX, S/T Bus Interface Circuit Extended, PEB 2081 V3.4, User's Manual 11.96, Siemens AG, 1996

[9] NTC-T, Network Termination Controller (4B3T), PEB 8090 V1.1, Data Sheet 06.98, Siemens AG, 1998

[10] INTC-Q, Intelligent Network Termination Controller (2B1Q), PEB 8191 V1.1, Data Sheet 10.97, Siemens AG, 1997

[11] Q-SMINTO, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(O**rdinary), PEF 80912
Q-SMINTIX, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(I**ntelligent e**X**tended), PEF 81912
Q-SMINTI, 2B1**Q** **S**econd Gen. **M**odular **I**SDN **NT** **(I**ntelligent), PEF 82912 V1.3, Data Sheets 03.01, Infineon AG, 2001

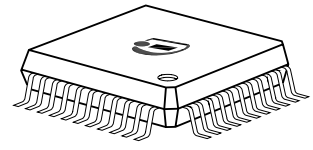
[12] IOM®-2 Interface Reference Guide, Siemens AG, 03.91

[13] SCOUT-S(X), Siemens Codec with S/T-Transceiver, PSB 2138x V1.1, Preliminary Data Sheet 08.98, Infineon Technologies AG, 1999

[14] PITA, PCI Interface for Telephony/Data Applications V0.3, SICAN GmbH, September1997

[15] Dual Channel SLICOFI-2, HV-SLIC; DUSLIC; PEB3265, 4265, 4266; Data Sheet DS2, Infineon Technologies, July 2000.

1.2 Features



P-MQFP-44

Features known from the PEB 8090

- Single chip solution including U- and S-transceiver
- Perfectly suited for the NT1 in the ISDN
- Fully automatic activation and deactivation
- U-interface (4B3T) conform to ETSI [1] and FTZ [2]:
  - Meets all transmission requirements on all ETSI and FTZ loops with margin
- S/T-interface conform to ETSI [4], ANSI [5] and ITU [6]
  - Supports point-to-point and bus configurations
  - Meets and exceeds all transmission requirements
- Optional IOM®-2 interface eases chip testing and evaluation
- Power-on reset and Undervoltage Detection with no external components
- ESD robustness 2kV

Type	Package
PEF 80902	P-MQFP-44

New Features

- Optional use of transformers with non-negligible resistance corresponding to up to 20Ω on the line sidePin Vref and the according external capacitor removed
- Inputs accept 3.3V and 5V
- I/O (open drain) accepts pull-up to 3.3V[1)]
- Pin compatible with Q-SMINT®O (2nd Generation)
- LEDs indicating Loopback 2 and activation status
- Lowest power consumption due to
  - Low power CMOS technology (0.35µ)
  - Newly optimized low power libraries
  - High output swing on U- and S-line interface leads to minimized power consumption
  - Single 3.3 Volt power supply
- 185mW (NTC-T: 233mW) power consumption with random data over ETSI Loop 2.
- 15mW typical power consumption in power down (as NTC-T; NTC-Q: 28mW)

1.3 Not Supported are ...

- No integrated hybrid is provided by the T-SMINT®O. Therefore, an external hybrid is always required, which consists of only two additional resistors as compared to an integrated hybrid, but allows for more flexibility in board design.
- Auxiliary IOM®–2 interface
- SRA (capacitive receiver coupling is not suited for S-feeding)
- NT-Star with star point on the IOM®-2 bus (already not supported in NTC-T).

1) Pull-ups to 5V must be avoided. A so-called 'hot-electron-effect' would lead to long term degradation.

1.4 Pin Configuration

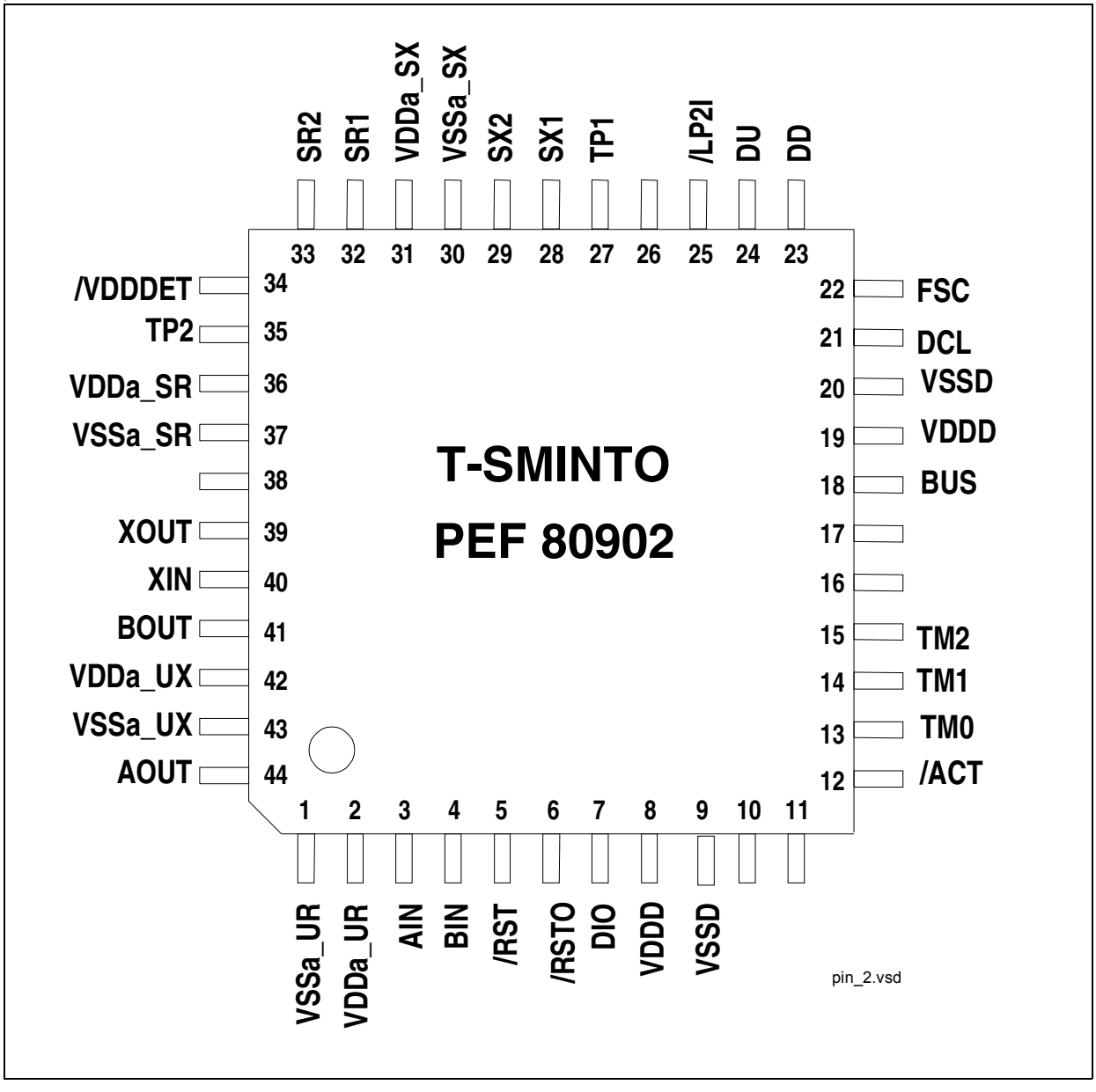


Figure 1 Pin Configuration

1.5 Block Diagram

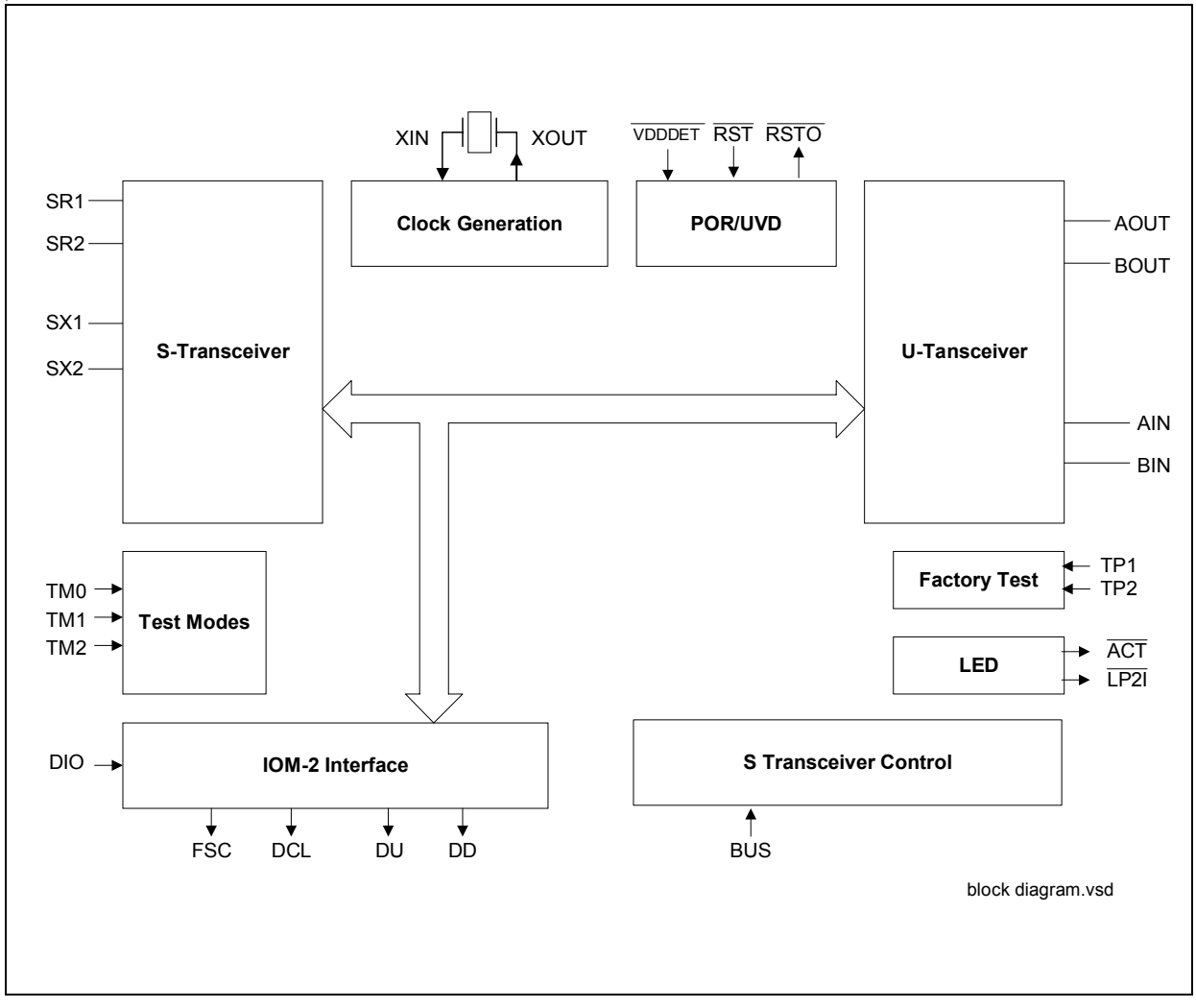


Figure 2 Block Diagram

1.6 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

Pin		Symbol	Type	Function
2		VDDa_UR	–	Supply voltage for U-Receiver (3.3 V ± 5 %)
1		VSSa_UR	–	Analog ground (0 V) U-Receiver
42		VDDa_UX	–	Supply voltage for U-Transmitter (3.3 V ± 5 %)
43		VSSa_UX	–	Analog ground (0 V) U-Transmitter
36		VDDa_SR	–	Supply voltage for S-Receiver (3.3 V ± 5 %)
37		VSSa_SR	–	Analog ground (0 V) S-Receiver
31		VDDa_SX	–	Supply voltage for S-Transmitter (3.3 V ± 5 %)
30		VSSa_SX	–	Analog ground (0 V) S-Transmitter
19		VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
20		VSSD	–	Ground (0 V) digital circuits
8		VDDD	–	Supply voltage digital circuits (3.3 V ± 5 %)
9		VSSD	–	Ground (0 V) digital circuits
22		FSC	O	**Frame Sync:** 8-kHz frame synchronization signal
21		DCL	O	**Data Clock:** IOM®-2 interface clock signal (double clock): 512 kHz
25		LP2I	O	**Loopback 2 indication:** Can directly drive a LED (4mA). 0: Loopback 2 closed 1: Loopback 2 not closed.
23		DD	I/O	**Data Downstream:** Data on the IOM®-2 interface

Table 2 Pin Definitions and Functions (cont'd)

Pin		Symbol	Type	Function
24		DU	I/O	**Data Upstream:** Data on the IOM®-2 interface
7		$\overline{\text{DIO}}$	I	Disable IOM®-2: 1: FSC, DCL, DU and DD high Z 0: FSC, DCL, DU and DD push-pull
18		BUS	I (PU)	**Bus mode on S-interface:** 1: passive S-bus (fixed timing) 0: point-to-point / extended passive S-bus (adaptive timing)
5		$\overline{\text{RST}}$	I	**Reset:** Low active reset input. Schmitt-Trigger input with hysteresis of typical 360mV. Tie to '1' if not used.
6		$\overline{\text{RSTO}}$	OD	**Reset Output:** Low active reset output.
13		TM0	I	**Test Mode 0.** Selects test pattern (see **Page 10**).
14		TM1	I	**Test Mode 1.** Selects test pattern (see **Page 10**).
15		TM2	I	**Test Mode 2.** Selects test pattern (see **Page 10**).
28		SX1	O	**S-Bus Transmitter Output (**positive**)**
29		SX2	O	**S-Bus Transmitter Output (**negative**)**
32		SR1	I	**S-Bus Receiver Input**
33		SR2	I	**S-Bus Receiver Input**
40		XIN	I	**Crystal 1:** Connected to a 15.36 MHz crystal
39		XOUT	O	**Crystal 2:** Connected to a 15.36 MHz crystal

Table 2 Pin Definitions and Functions (cont'd)

Pin		Symbol	Type	Function
44		AOUT	O	**Differential U-interface Output**
41		BOUT	O	**Differential U-interface Output**
3		AIN	I	**Differential U-interface Input**
4		BIN	I	**Differential U-interface Input**
34		$\overline{\text{VDDDET}}$	I	**VDD Detection:** This pin selects if the V_{DD} detection is active ('0') and reset pulses are generated on pin $\overline{\text{RSTO}}$ or whether it is deactivated ('1') and an external reset has to be applied on pin $\overline{\text{RST}}$.
12		$\overline{\text{ACT}}$	O	**Activation LED.** Indicates the activation status of U- and S-transceiver. Can directly drive a LED (4mA).
27		TP1	I	**Test Pin 1.** Used for factory device test. Tie to 'V_{SS}'
35		TP2	I	**Test Pin 2.** Used for factory device test. Tie to 'V_{SS}'
10,11, 16,17, 26,38				Tie to '1'

PU: Internal pull-up resistor (typ. 100µA)

I: Input

O: Output (Push-Pull)

OD: Output (Open Drain)

1.6.1 Specific Pins and Test Modes

LED Pins $\overline{\text{ACT}}$, $\overline{\text{LP2I}}$

A LED can be connected to pin **$\overline{\text{ACT}}$** to display four different states (off, slow flashing, fast flashing, on). It displays the activation status of the U- and S-transceiver according to **Table 3**.

Table 3 ACT States

Pin $\overline{ACT}$	LED	U_Deactivated	U_Activated	S_Activated
V_{DD}	OFF	1	x	x
2Hz (1 : 1)*	fast flashing	0	0	x
1Hz (3 : 1)*	slow flashing	0	1	0
GND	ON	0	1	1

Note: * denotes the duty cycle 'high' : 'low'.

with:

U_Deactivated: 'Deactivated State' as defined in **Chapter 2.3.7.6**.

U_Activated: 'SBC Synchronizing', 'Wait for Info U4H', and 'Transparent' as defined in **Chapter 2.3.7.6**.

S-Activated: 'Activated State' as defined in **Chapter 2.4.5.1**.

Note: Optionally, pin $\overline{ACT}$ can drive a second LED with inverse polarity (connect this additional LED to 3.3V only).

Another LED can be connected to pin **$\overline{LP2I}$** to indicate an active Loopback 2 according to **Table 4.**

Table 4 LP2I States

Pin $\overline{LP2I}$	LED	Loopback 2 command in the C_L -channel
V_{DD}	off	received no loopback 2 command or loopback deactivation after a loopback 2 command.
GND	on	Loopback 2 command has been received. Complete analog loop is being closed on the S-interface.

Test Modes

Different test patterns on the U- and S-interface can be generated via pins TM0-2 according to **Table 5**.

Table 5 Test Modes

TM0	TM1	TM2	U-transceiver	S-transceiver
0	0	0	Reserved for future use. Normal operation in this version.	
0	0	1		
0	1	0	Normal operation	96 kHz[1)] Continuous Pulses
0	1	1		2 kHz[2)] Single Pulses

Table 5 Test Modes (cont'd)

TM0	TM1	TM2	U-transceiver	S-transceiver
1	0	0	Data Through[3]	Normal operation
1	0	1	Send Single Pulses[4]	
1	1	0	Quiet Mode[5]	
1	1	1	normal operation	

1) The S-transceiver transmits pulses with alternating polarity at a rate of 192 kHz resulting in a 96 kHz envelope.

2) The S-transceiver transmits pulses with alternating polarity at a rate of 4 kHz resulting in a 2 kHz envelope.

3) Forces the U-transceiver into the state 'Transparent' where it transmits signal U5.

4) Forces the U-transceiver to go into state 'Test' and to send single pulses. The pulses are issued at 1.0 ms intervals and have a duration of 8.33 µs.

5) The U-transceiver is hardware reset.

1.7 System Integration

The T-SMINT®O provides NT1 functionality without a microcontroller being necessary. Special selections can be done via pin strapping (DIO, BUS, TM0-2). The device has no µP interface.

The IOM®-2 Interface serves only for monitoring and debugging purposes. It can be regarded as a window to the internal IOM®-2.

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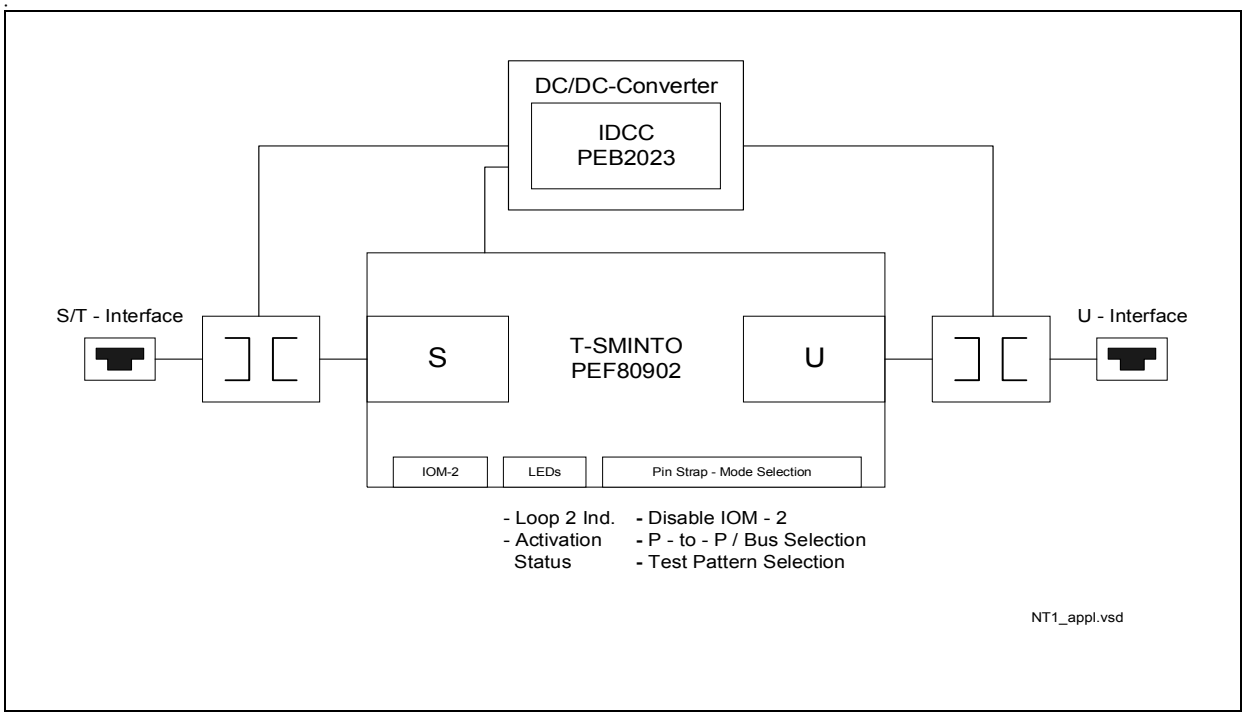


Figure 3 Application Example T-SMINT®O: Standard NT1

2 Functional Description

2.1 Reset Generation

External Reset Input

At the $\overline{\text{RST}}$ input an external reset can be applied forcing the T-SMINT®O in the reset state. This external reset signal is additionally fed to the $\overline{\text{RSTO}}$ output.

Reset Ouput

If $\overline{\text{VDDDET}}$ is active, then the deactivation of a reset output on $\overline{\text{RSTO}}$ is delayed by t_{DEACT} (see **Table 28**).

Reset Generation

The T-SMINT®O has an on-chip reset generator based on a Power-On Reset (POR) and Under Voltage Detection (UVD) circuit (see **Table 28**). The POR/UVD requires no external components.

The POR/UVD circuit can be disabled via pin $\overline{\text{VDDDET}}$.

The requirements on V_{DD} ramp-up during power-on reset are described in **Chapter 4.6.3**.

Clocks and Data Lines During Reset

During reset the data clock (DCL) and the frame synchronization (FSC) keep running.

During reset DD and DU are high; with the exception of:

- The output C/I code from the U-Transceiver on DD is 'DR' = 0000
- The output C/I code from the S-Transceiver on DU is 'TIM' = 0000.

2.2 IOM®-2 Interface

The IOM®-2 interface always operates in NT mode according to the IOM®-2 Reference Guide [12].

2.2.1 IOM®-2 Functional Description

The IOM®-2 interface consists of four lines: FSC, DCL, DD, DU. The rising edge of FSC indicates the start of an IOM®-2 frame. The DCL clock signal synchronizes the data transfer on both data lines DU and DD. The DCL is twice the bit rate. The bits are shifted out with the rising edge of the first DCL clock cycle.

Note: It is not possible to write any data via IOM®-2 into the T-SMINT®O.

The IOM®-2 interface can be enabled/disabled with pin DIO.

The FSC signal is an 8 kHz frame sync signal. The number of PCM timeslots on the transmit line is determined by the frequency of the DCL clock , with the 512 kHz clock 1 channel consisting of 4 timeslots is available.

IOM®-2 Frame Structure of the T-SMINT®O

The frame structure on the IOM®-2 data ports (DU,DD) of the T-SMINT®O with a DCL clock of 512 kHz is shown in **Figure 4.**

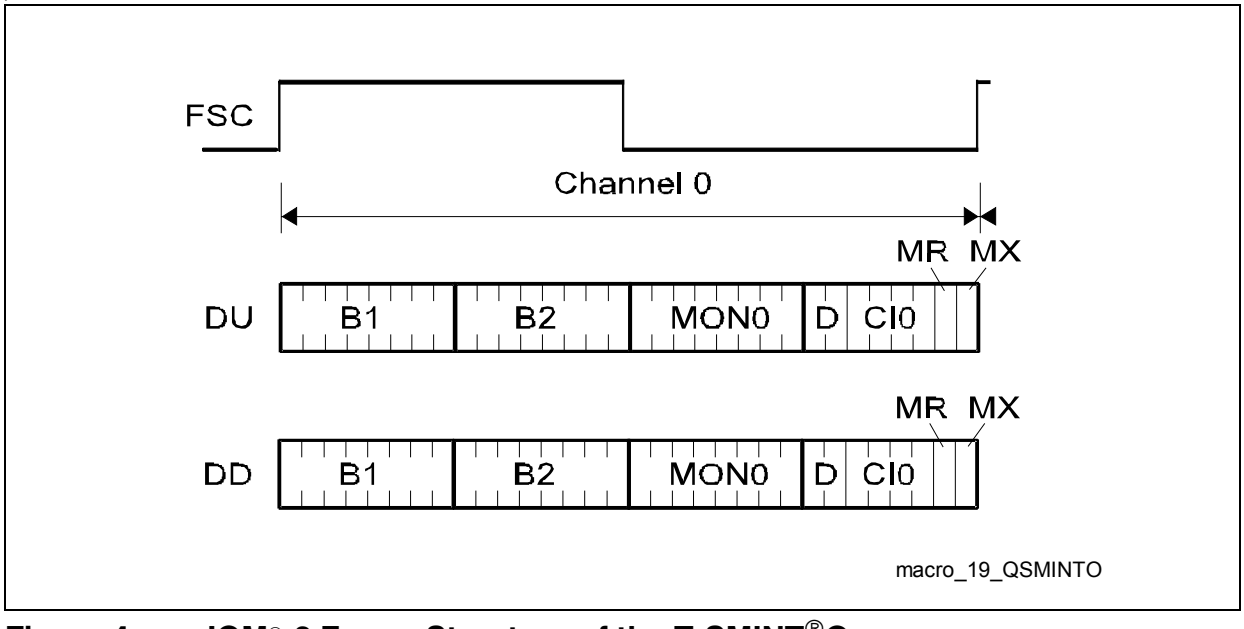


Figure 4 IOM®-2 Frame Structure of the T-SMINT®O

The frame is composed of one channel:

- Channel 0 contains 144-kbit/s of user and signaling data (2B + D), a MONITOR programming channel (not available in T-SMINT®O) and a command/indication channel (CI0) for control of e.g. the U-transceiver.

2.3 U-Transceiver

The statemachine of the U-Transceiver is compatible to the NT state machine in the PEB 8090 documentation [9], but includes some minor changes for simplification and compliance to Ref. [1].

Basic configurations are selected via pin strapping

2.3.1 4B3T Frame Structure

The 4B3T U-interface performs full duplex data transmission and reception at the U-reference point according to ETSI TS 102 080 and FTZ 1TR 220. It applies the 4B3T block code together with adaptive echo cancelling and equalization. Transmission performance shall be such, that it meets all ETSI and FTZ test loops with margin.

The U-interface is designed for data transmission on twisted pair wires in local telephone loops, with basic access to ISDN and a user bit rate of 144 kbit/s.

The following information is transmitted over the twisted pair:

- Bidirectional:
  - B1, B2, D data channels
  - 120 kHz Symbol clock
  - 1 kHz Frame
  - Activation
  - 1 kbit/s Transparent Channel (M symbol), (not implemented)
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops (M symbol)
- From NT to LT side:
  - Indication of monitored code violations (M symbol)

Performance Requirements according to FTZ 1 TR 220 (August 1991):

On the U-interface, the following transmission ranges are achieved without additional signal regeneration on the loop (bit error rate $\leq 10^{-7}$):

- with noise: ≥ 4.2 km on wires of 0.4 mm diameter and ≥ 8 km on 0.6 mm wires
- without noise: ≥ 5 km on wires of 0.4 mm diameter and ≥ 10 km on 0.6 mm wires

Note: Typical attenuation of FTZ wires of 0.4 mm diameter is about 7dB/km in contrast to ETSI wires of 0.4 mm with about 8dB/km.

The transmission ranges can be doubled by inserting a repeater for signal regeneration.

Performance requirements according to ETSI TS 102 080 are met, too.

1 ms frames are transmitted via the U-interface, each consisting of:

- 108 symbols: 144 bit scrambled and coded B1 + B2 + D data

- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, resp. 36 bits) contains the user data of two IOM®-2 frames in the same order (8B + 8B + 2D + 8B + 8B + 2D).

Different syncwords are used for each direction:

- Downstream from LT to NT + + + – – – + – – + –
- Upstream from NT to LT – + – – + – – – + + +

On the NT side, the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

Table 6 Frame Structure A for Downstream Transmission LT to NT

1 D_1	2 D_1	3 D_1	4 D_1	5 D_1	6 D_1	7 D_1	8 D_1	9 D_1	10 D_1	11 D_1	12 D_1
13 $D_{1/2}$	14 $D_{1/2}$	15 $D_{1/2}$	16 D_2	17 D_2	18 D_2	19 D_2	20 D_2	21 D_2	22 D_2	23 D_2	24 D_2
25 D_2	26 D_2	27 D_2	28 D_3	29 D_3	30 D_3	31 D_3	32 D_3	33 D_3	34 D_3	35 D_3	36 D_3
37 D_3	38 D_3	39 D_3	40 $D_{3/4}$	41 $D_{3/4}$	42 $D_{3/4}$	43 D_4	44 D_4	45 D_4	46 D_4	47 D_4	48 D_4
49 D_4	50 D_4	51 D_4	52 D_4	53 D_4	54 D_4	55 D_5	56 D_5	57 D_5	58 D_5	59 D_5	60 D_5
61 D_5	62 D_5	63 D_5	64 D_5	65 D_5	66 D_5	67 $D_{5/6}$	68 $D_{5/6}$	69 $D_{5/6}$	70 D_6	71 D_6	72 D_6
73 D_6	74 D_6	75 D_6	76 D_6	77 D_6	78 D_6	79 D_6	80 D_6	81 D_6	82 D_7	83 D_7	84 D_7
85 **M**	86 D_7	87 D_7	88 D_7	89 D_7	90 D_7	91 D_7	92 D_7	93 D_7	94 D_7	95 $D_{7/8}$	96 $D_{7/8}$
97 $D_{7/8}$	98 D_8	99 D_8	100 D_8	101 D_8	102 D_8	103 D_8	104 D_8	105 D_8	106 D_8	107 D_8	108 D_8
109 D_8	110 **+**	111 **+**	112 **+**	113 **–**	114 **–**	115 **–**	116 **+**	117 **–**	118 **–**	119 **+**	120 **–**

D_1 ... D_8	Ternary 2B + D data of IOM®-2 frames 1 ... 8
M	Maintenance symbol
+, –	Syncword

Table 7 Frame Structure B for Upstream Transmission NT to LT

1 U_1	2 U_1	3 U_1	4 U_1	5 U_1	6 U_1	7 U_1	8 U_1	9 U_1	10 U_1	11 U_1	12 U_1
13 $U_{1/2}$	14 $U_{1/2}$	15 $U_{1/2}$	16 U_2	17 U_2	18 U_2	19 U_2	20 U_2	21 U_2	22 U_2	23 U_2	24 U_2
25 **M**	26 U_2	27 U_2	28 U_2	29 U_3	30 U_3	31 U_3	32 U_3	33 U_3	34 U_3	35 U_3	36 U_3
37 U_3	38 U_3	39 U_3	40 U_3	41 $U_{3/4}$	42 $U_{3/4}$	43 $U_{3/4}$	44 U_4	45 U_4	46 U_4	47 U_4	48 U_4
49 U_4	50 –	51 +	52 –	53 –	54 +	55 –	56 –	57 –	58 +	59 +	60 +
61 U_4	62 U_4	63 U_4	64 U_4	65 U_4	66 U_4	67 U_5	68 U_5	69 U_5	70 U_5	71 U_5	72 U_5
73 U_5	74 U_5	75 U_5	76 U_5	77 U_5	78 U_5	79 $U_{5/6}$	80 $U_{5/6}$	81 $U_{5/6}$	82 U_6	83 U_6	84 U_6
85 U_6	86 U_6	87 U_6	88 U_6	89 U_6	90 U_6	91 U_6	92 U_6	93 U_6	94 U_7	95 U_7	96 U_7
97 U_7	98 U_7	99 U_7	100 U_7	101 U_7	102 U_7	103 U_7	104 U_7	105 U_7	106 $U_{7/8}$	107 $U_{7/8}$	108 $U_{7/8}$
109 U_8	110 U_8	111 U_8	112 U_8	113 U_8	114 U_8	115 U_8	116 U_8	117 U_8	118 U_8	119 U_8	120 U_8

U_1 ... U_8 Ternary 2B + D data of IOM®-2 frames 1... 8

M Maintenance symbol

+, - Syncword

2.3.2 Maintenance Channel

The 4B3T frame structure provides a 1 kbit/s M(aintenance)-channel for the transfer of remote loopback commands and error indications.

Loopback Commands

The LT station uses the M-channel to request remote loopbacks. Loopback commands are coded with a series of ’0’ and ’+’ symbols.

- A continuous series of ’+’ requests for loopback 2 activation in the NT
- A continuous series of ’0’ requests for deactivation of any loopback

The NT station reacts as soon as the pattern has been detected in 8 consecutive symbols.

Error Indications

The NT U-transceiver reports line code violations via the M-channel to the exchange by setting one M-Bit to ’+’ polarity.

Transparent Messages

The exchange of Transparent Messages via the Transparent Channel is not supported by the T-SMINTO.

2.3.3 Coding from Binary to Ternary Data

Each 4 bit block of binary data is coded into 3 ternary symbols of MMS 43 block code according to **Table 8**.

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

Table 8 MMS 43 Coding Table

				S1				S2				S3				S4			
t →				t →				t →				t →				t →			
0	0	0	1	0	–	+	1	0	–	+	2	0	–	+	3	0	–	+	4
0	1	1	1	–	0	+	1	–	0	+	2	–	0	+	3	–	0	+	4
0	1	0	0	–	+	0	1	–	+	0	2	–	+	0	3	–	+	0	4
0	0	1	0	+	–	0	1	+	–	0	2	+	–	0	3	+	–	0	4
1	0	1	1	+	0	–	1	+	0	–	2	+	0	–	3	+	0	–	4
1	1	1	0	0	+	–	1	0	+	–	2	0	+	–	3	0	+	–	4
1	0	0	1	+	–	+	2	+	–	+	3	+	–	+	4	–	–	–	1

Table 8 MMS 43 Coding Table (cont'd)

				S1				S2				S3				S4			
0	0	1	1	0	0	+	2	0	0	+	3	0	0	+	4	–	–	0	2
1	1	0	1	0	+	0	2	0	+	0	3	0	+	0	4	–	0	–	2
1	0	0	0	+	0	0	2	+	0	0	3	+	0	0	4	0	–	–	2
0	1	1	0	–	+	+	2	–	+	+	3	–	–	+	2	–	–	+	3
1	0	1	0	+	+	–	2	+	+	–	3	+	–	–	2	+	–	–	3
1	1	1	1	+	+	0	3	0	0	–	1	0	0	–	2	0	0	–	3
0	0	0	0	+	0	+	3	0	–	0	1	0	–	0	2	0	–	0	3
0	1	0	1	0	+	+	3	–	0	0	1	–	0	0	2	–	0	0	3
1	1	0	0	+	+	+	4	–	+	–	1	–	+	–	2	–	+	–	3

2.3.4 Decoding from Ternary to Binary Data

Decoding is done in the reverse manner of coding. The received blocks of 3 ternary symbols are converted into blocks of 4 bits. The decoding algorithm is given in **Table 9**.

As in the encoding table, the left hand symbol of each block (both binary and ternary) is the first bit and the right hand is the last. If a ternary block "0 0 0" is received, it is decoded to binary "0 0 0 0". This pattern usually occurs only during deactivation.

Table 9 4B3T Decoding Table

Ternary Block			Binary Block			
0 0 0,	+ 0 +,	0 – 0	0	0	0	0
0 – +			0	0	0	1
+ – 0			0	0	1	0
0 0 +,	– – 0		0	0	1	1
– + 0			0	1	0	0
0 + +,	– 0 0		0	1	0	1
– + +,	– – +		0	1	1	0
– 0 +			0	1	1	1
+ 0 0,	0 – –		1	0	0	0
+ – +,	– – –		1	0	0	1
+ + –,	+ – –		1	0	1	0
+ 0 –			1	0	1	1
+ + +,	– + –		1	1	0	0

Table 9 4B3T Decoding Table (cont'd)

0 + 0,	– 0 –	1	1	0	1
0 + –		1	1	1	0
+ + 0,	0 0 –	1	1	1	1

2.3.4.1 Monitoring of Code Violations

The running digital sum monitor (RDSM) computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+ 1, 0, –1). At the end of each block, the running digital sum is supposed to reflect the number of the next column in **Table 8.**

A code violation has occurred if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0 (three user symbols with zero polarity) is found in the received data.

If at the end of a ternary block no error was found, the running digital sum retains its current value. If the counter value is greater than 4, it is set to 4 at the beginning of the next ternary block, if its value is 0 or less, it is set to one. So after a code violation has been detected, the RDSM synchronizes itself within a period depending on the received data pattern. Note there are some transmission errors which do not cause a code violation.

2.3.5 Scrambler / Descrambler

Scrambler

The binary transmit data from the IOM®-2 interface is scrambled with a polynomial of 23 bits, before it is sent to the 4B3T coder. The scrambler polynomial is::

$$z^{-23} + z^{-18} + 1$$

Descrambler

The received data (after decoding from ternary to binary) is multiplied with a polynomial of 23 bits in order to recover the original data before it is forwarded to the IOM®-2 interface.The descrambler is self synchronized after 23 symbols. The descrambler polynomial is::

$$z^{-23} + z^{-5} + 1$$

The scrambling / descrambling process is controlled fully by the T-SMINTO. Hence, no influence can be taken by the user.

2.3.6 Command/Indication Codes

Both commands and indications depend on the data direction. **Table 10** presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM®-2 frames (double last-look criterion).

Indications are strictly state orientated. Refer to the state diagrams in the following sections for commands and indications applicable in various states.

Table 10 C/I Codes

Code	IN	OUT
0000	TIM	DR
0001	–	–
0010	–	–
0011	LTD	–
0100	–	RSY
0101	SSP	–
0110	DT	–
0111	–	–
1000	AR	AR
1001	reserved[1)]	–
1010	–	ARL
1011	–	–
1100	AI	AI
1101	RES	–
1110	–	AIL
1111	DI	DC

1) C/I code ‘1010‘ must not be input to the U-transceiver.

.

AI	Activation Indication	DI	Deactivation Indication.
AIL	Activation Indication Loop 2	DR	Deactivation Request
AR	Activation Request	LTD	LT Disable
ARL	Activation Request Local Loop	RES	Reset
DT	Data Through Mode	RSY	Resynchronization Indication

DC	Deactivation Confirmation	SSP	Send-Single-Pulses
		TIM	Timing Request

2.3.7 State Machine for Activation and Deactivation

2.3.7.1 State Machine Notation

The following state diagram describes all the actions/reactions resulting from any command or detected signal and resulting from the various operating modes.

The states with its inputs and outputs are interpreted as shown below:

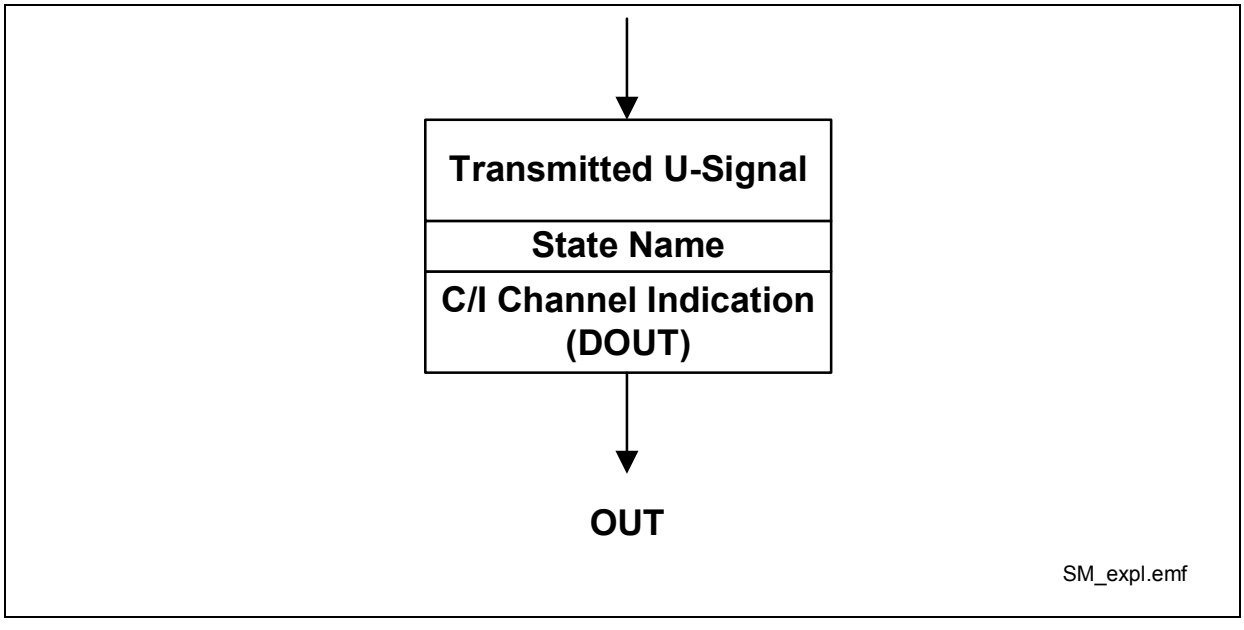


Figure 5 State Diagram Example

Each state has one or more transitions to other states. These transitions depend on certain conditions which are noted next to the transition lines. These conditions are the only possibility to leave a state. If more conditions have to be fulfilled together, they are put into parentheses with an AND operator (&). If more than one condition leads to the same transition, they are put into parentheses with an OR operator (|). The meaning of a condition may be inverted by the NOT operator (/). Only the described states and transitions exist.

At some transitions, an internal timer is started. The start of a timer is indicated by TxS ('x' is the timer number). Transitions that are caused if a timer has expired are labelled by TxE.

Some conditions lead to the same target state. To reduce the number of lines and the complexity of the figures, a state named "ANY STATE" acts on behalf of all state.

The state machines are designed to cope with all ISDN devices with IOM®-2 standard interfaces. Undefined situations are excluded. In any case, the involved devices will enter defined conditions as soon as the line is deactivated.

2.3.7.2 Awake Protocol

For the awake process two signals are defined' U1W' and 'U2W'. Depending on the call direction (up-, downstream) U1W and U2W are interpreted as awake or acknowledge signals (see figures below).

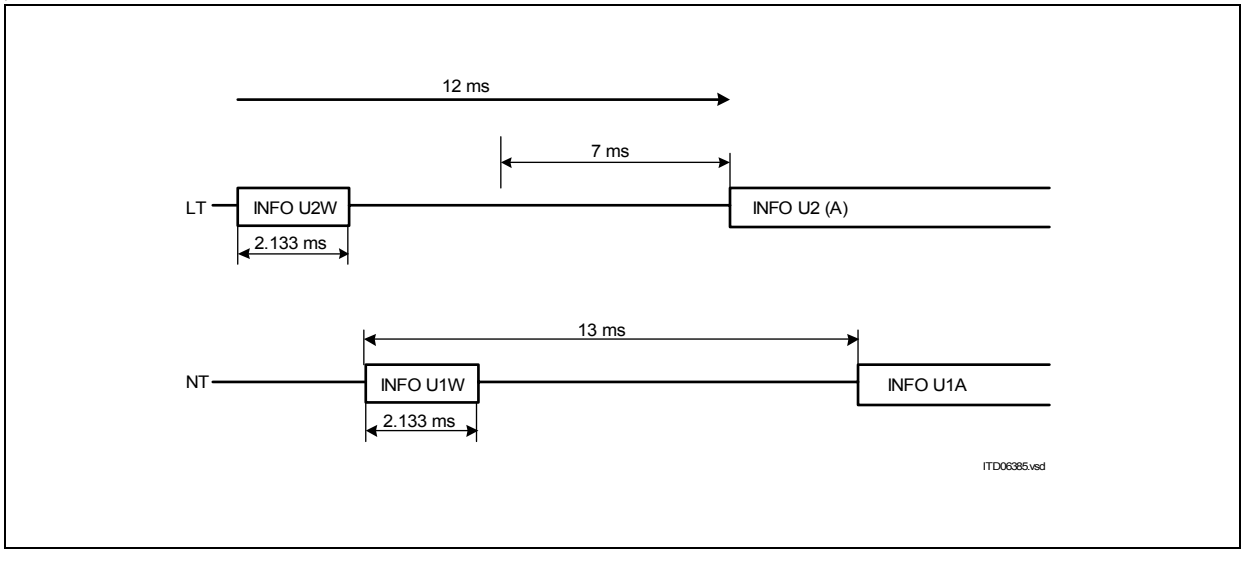


Figure 6 Awake Procedure initiated by the LT

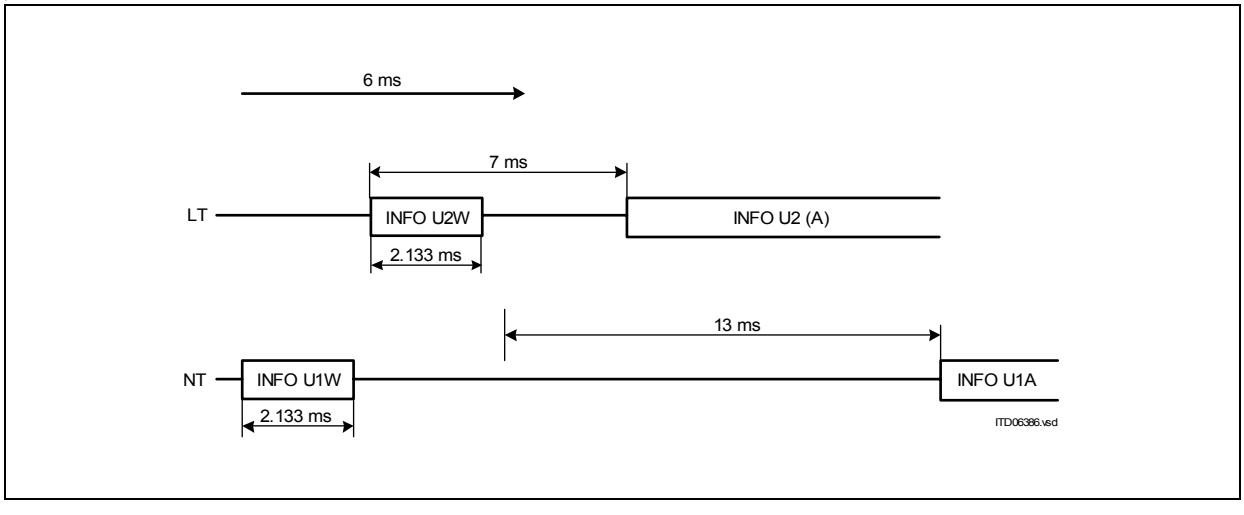


Figure 7 Awake Procedure initiated by the NT

Acting as Calling Station

After sending the awake signal, the awaking U-transceiver waits for the acknowledge. After 12 ms, the awake signal is repeated, if no acknowledge has been recognized.

If an acknowledge signal has been recognized, the U-transceiver waits for its possible repetition (in case of previous coincidence of two awake signals). If no repetition was detected, the U-transceiver starts transmitting U2 with a delay of 7 ms.

If such a repetition is detected, the U-transceiver interprets it as an awake signal and behaves like a device awoken by the far end.

Acknowledging a Wake-Up Call

If a deactivated device detects an awake signal on U, an acknowledge signal is sent out. After that, the U-transceiver waits for a possible repetition of the awake signal (in case the acknowledge hasn't been recognized).

If no repetition is found, the awoken U-transceiver starts sending U2 after 7 ms from detecting the awake signal. If a repeated awake signal is found, the procedure in the awoken U-transceiver starts again.

2.3.7.3 NT State Machine (IEC-T / NTC-T Compatible)

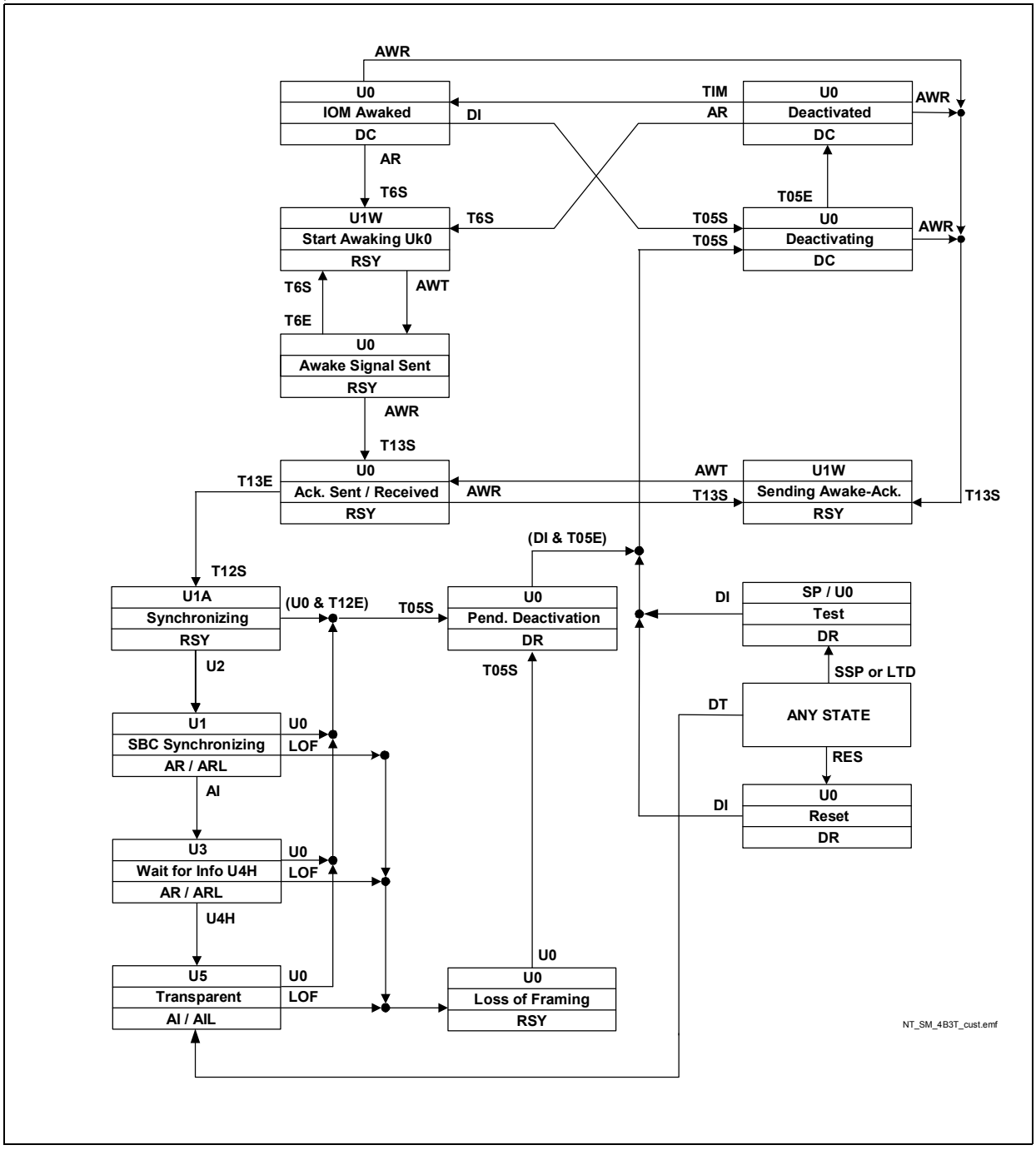


Figure 8 NT State Machine (IEC-T/NTC-T Compatible)

Note: The test modes 'Data Through' (DT), 'Send Single Pulses' (SSP) and 'Quiet Mode' (QM) can be generated via pins TM0-2 according to **Table 5**.

Table 11 Differences to the former NT-SM of the IEC-T/NTC-T

No.	State/ Signal	Change	Comment
1.	State 'Deact. Request Rec.'	split into 3 states - 'Pend. Deactivation 1' - 'Reset' State - 'Test' State	simplifies SM implementation
2.	State 'Loss of Framing'	new inserted, results in different behavior in state 'Transparent', no return to normal transmission possible after detection of LOF	compliance to ETSI TS 102 080, corresponds to state NT1.10
3.	C/I-code LTD	new inserted	
4.	State 'Power Down'	renamed to state 'Deactivated'	for consistency reasons to 2B1Q
5.	State 'Data Transmission'	renamed to state 'Transparent'	
6.	Timer variables introduced	Name Duration	see **Table 12**

2.3.7.4 Inputs to the U-Transceiver

C/I-Commands

AI Activation Indication
The downstream device issues this indication to announce that layer 1 is available. The U-transceiver in turn informs the LT side by transmitting U3.

AR Activation Request
The U-transceiver is requested to start the activation process (if not already done) by sending the wake-up signal U1W.

DI Deactivation Indication
This indication is used during a deactivation procedure to inform the U-transceiver that it may enter the 'Deactivated' (power-down) state.

DT Data Through Test Mode
This unconditional command is used for test purposes only and forces the U-transceiver into state 'Transparent'.

LTD LT Disable
This unconditional command forces the U-transceiver to state 'Test', where it transmits U0. No further action is initiated.

RES Reset
Unconditional command which resets the U-transceiver.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface.

TIM Timing
The U-transceiver is requested to enter state 'IOM Awaked'.

U-Interface Events

U0 U0 detected
U0 is recognized after 120 symbols (1ms) with zero level in a row. Detection may last up to 2 ms.

U2 U2 detected
The U-transceiver detects U2 if continuous binary 0's are found after descrambling and LOF = 0 for at least 8 subsequent U-frames. U2 is detected after 8 to 9 ms.

U4H U4H detected
U4H is recognized, if the U-transceiver detects 16 subsequent binary 1's after descrambling.

AWR Awake signal (U2W) detected

AWT Awake signal (U1W) has been sent out

LOF Loss of Framing on U-interface

TxE Timer ended, the started timer has expired

Timers

The start of timers is indicated by TxS, the expiry by TxE. The following table shows which timers are used.

Table 12 Timers

Timer	Duration (ms)	Function	State
T05	0.5	C/I code recognition	Pend. Deactivation, Deactivating
T6	6	Supervises U1W repetition	Start Awaking Uk0

Table 12 Timers (cont'd)

Timer	Duration (ms)	Function	State
T12	12	Prevents the U-transceiver in state Synchronizing from immediate transition to state 'Pend. Deactivation' if U0 is detected	Synchronizing
T13	13	Supervises U2W repetition	Ack. sent / received Sending awake-ack.

2.3.7.5 Outputs of the U-Transceiver

Below the signals and indications are summarized that are issued on IOM®-2 (C/I indications) and on the U-interface (predefined U-signals).

C/I Indications

AI Activation Indication
The U-transceiver has established transparency of transmission. The downstream device is requested to establish layer-1 functionality.

AIL Activation Indication Loop-back
The U-transceiver has established transparency of transmission. The downstream device is requested to establish a loopback #2.

AR Activation Request
The downstream device is requested to start the activation procedure.

ARL Activation Request Loop-back
The U-transceiver has detected a loop-back 2 command in the M-channel and has established transparency of transmission in the direction IOM® to U-interface. The downstream device is requested to start the activation procedure and to establish a loopback #2.

DC Deactivation Confirmation
Idle code on the IOM®-2 interface.

DR Deactivation Request
The U-transceiver has detected a deactivation request command from the LT-side for a complete deactivation. The downstream device is requested to start the deactivation procedure.

RSY Resynchronizing Indication
RSY informs the downstream device that the U-transceiver is not synchronous.

Signals on U-Interface

The signals U0, U1W, U1A, U1, U3, U5 and SP are transmitted on the U-interface.They are defined in **Table 17**.

Signals on IOM®-2

The Data (B+B+D) is set to all ’1’s in all states besides the states listed in **Table 13**.

Table 13 Active States

SBC Sychronizing
Wait for INFO U4H
Transparent

Dependence of Outputs

The M-symbol output in states with valid M-symbol output its value is set according to **Table 14**

Table 14 M Symbol Output

RDS Error	not detected	detected
M Symbol Output	’0’	’+’

Table 15 Signal Output on Uk0 in State Test

Input	SSP active	all other except C/I-Code ’DI’
Signal Output on Uk0	SP	U0

Table 16 C/I-Code Output

Loopback Command	SBC Synchronizing	Wait for Info U4H	Transparent
not received	AR	AR	AI
received	ARL	ARL	AIL

2.3.7.6 NT-States

In this section each state is described with its function.

Acknowledge Sent / Receive

After having sent the awake signal, the U-transceiver has received the acknowledge wake tone. If being awoken the U-transceiver has sent the acknowledge. In both cases the U-transceiver waits for possible repetition or time-out.

Awake Signal Sent

The NT has sent out the awake signal U1W and waits now for a response. If the LT does not react in time timer T6 expires and the NT repeats its wake-up call.

Deactivated

Only in “Deactivated” state the device may enter the power-down mode.

Deactivating

State Deactivating assures that the C/I-channel code DC is issued four times before entering the ’Deactivated’ state.

IOM® Awaked

The U-transceiver is deactivated, but may not enter the power-down mode.

Loss of Framing

This state is entered on loss of framing (LOF). No signal is transmitted on the U-interface. A receiver-reset is performed by.

Note that there is no return to the ’Transparent’ state that has been possible before in the former IEC-T based state machine.

Pending Deactivation

The U-transceiver has received U0. The U-transceiver remains at least 0.5ms in this state before it accepts DI.

SBC Synchronizing

The NT is now synchronized and indicates this by AR/ARL towards the downstream device. The NT waits for the acknowledge ’AI’ from the downstream device.

Sending Awake-Ack.

On the receipt of the awake signal U2W the U-transceiver responds with the transmission of U1W.

Start Awaking Uk0

On the receipt of AR in the C/I-channel the U-transceiver sends the awake signal U1W to start an activation.

Synchronizing

After the successful awake procedure the U-transceiver trains its receiver coefficients until it is able to detect the signals U2.

Reset

In state 'Reset' a software-reset is performed.

Test

State "Test" is entered when the unconditional commands TM2-0='SSP' is applied. The test signal SSP is issued as long as pin SSP is active or C/I=SSP is applied.

Transparent

The transmission line is fully activated. User data is transparently exchanged by U4/U5. Transparent state is entered in the case of a loopback 2. The downstream device is informed by C/I code AI that the transparent state has been reached

Note that in contrast to the former IEC-T state machine there is no resynchronization mechanism. Once loss of framing (LOF) has been detected a deactivation is initiated.

Wait for Info U4H

The NT is synchronized and waits now for the permission (U4H) to go to the 'Transparent' state.

2.4 S-Transceiver

The S-Transceiver offers the NT state machine described in the User's Manual V3.4 [8].

The S-transceiver basic configurations are performed via pin strapping.

2.4.1 Line Coding, Frame Structure

Line Coding

The following figure illustrates the line code. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with two exceptions:
For the required frame structure a code violation is indicated by two consecutive pulses of the same polarity. These two pulses can be adjacent or separated by binary ONEs.
In bus configurations a binary ZERO always overwrites a binary ONE.

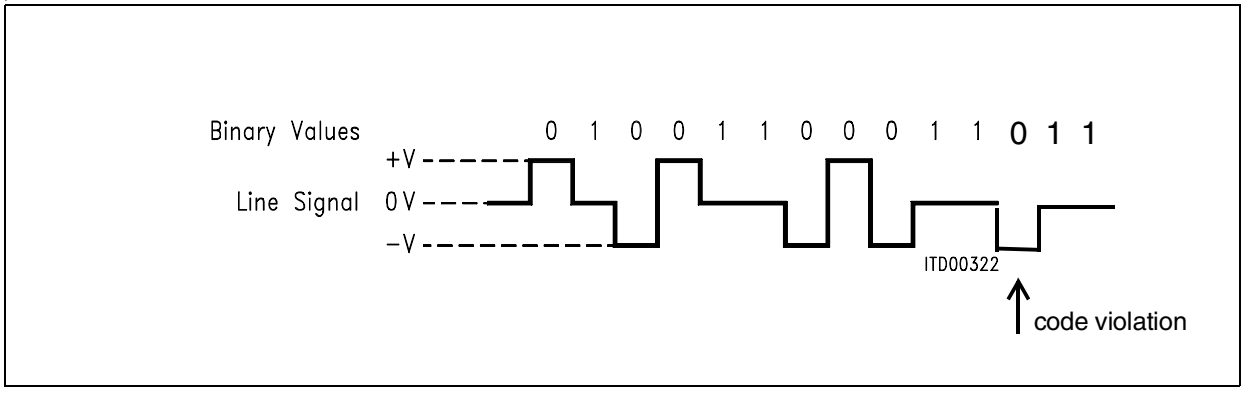


Figure 9 S/T -Interface Line Code

Frame Structure

Each S/T frame consists of 48 bits at a nominal bit rate of 192 kbit/s. For user data (B1+B2+D) the frame structure applies to a data rate of 144 kbit/s (see **Figure 9**).
In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

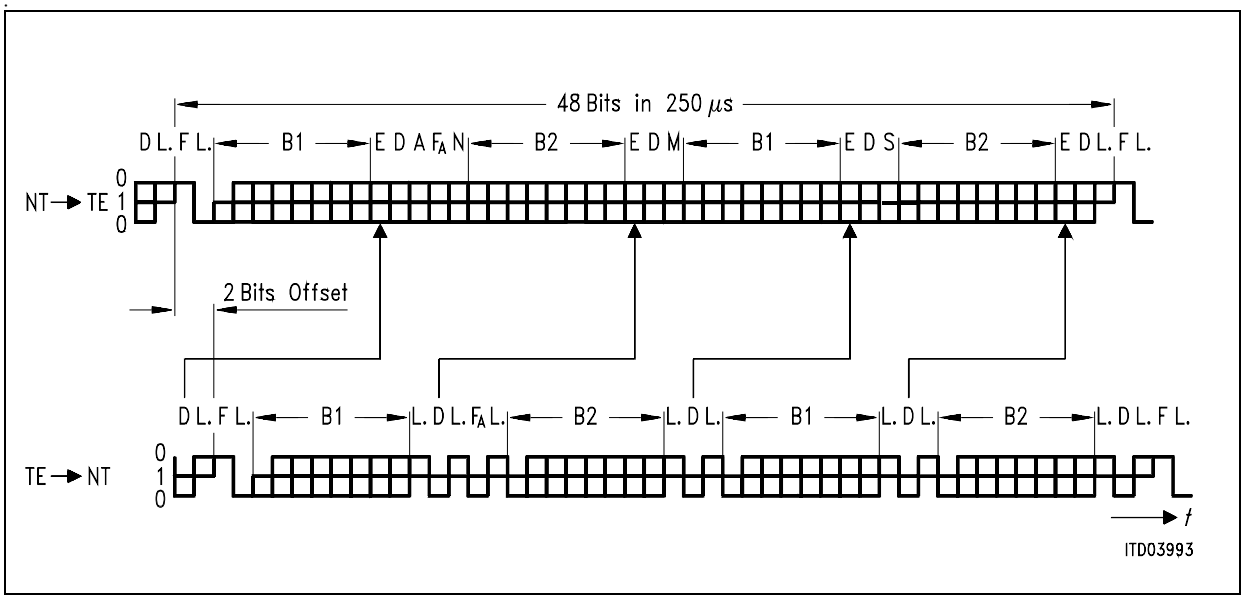


Figure 10 Frame Structure at Reference Points S and T (ITU I.430)

– F	Framing Bit	F = (0b) → identifies new frame (always positive pulse, always code violation)
– L.	D.C. Balancing Bit	L. = (0b) → number of binary ZEROs sent after the last L. bit was odd
– D	D-Channel Data Bit	Signaling data specified by user
– E	D-Channel Echo Bit	E = D → received E-bit is equal to transmitted D-bit
– F_A	Auxiliary Framing Bit	See section 6.3 in ITU I.430
– N		N = $\overline{F_A}$
– B1	B1-Channel Data Bit	User data
– B2	B2-Channel Data Bit	User data
– A	Activation Bit	A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
– S	S-Channel Data Bit	S_1 channel data (see note below)
– M	Multiframing Bit	M = (1b) → Start of new multi-frame

Note: The ITU I.430 standard specifies S1 - S5 for optional use.

2.4.2 S/Q Channels, Multiframing

The S/Q channels are not supported.

2.4.3 Data Transfer between IOM®-2 and S_0

In the state G3 (Activated) the B1, B2 and D bits are transferred transparently from the S/T to the IOM®-2 interface and vice versa. In all other states ’1’s are transmitted to the IOM®-2 interface.

2.4.4 Loopback 2

C/I commands ARL and AIL close the analog loop as close to the S-interface as possible. ETSI refers to this loop under ’loopback 2’. ETSI requires, that B1, B2 and D channels have the same propagation delay when being looped back.

The D-channel Echo bit is set to bin. 0 during an analog loopback (i.e. loopback 2). The loop is transparent.

Note: After C/I-code AIL has been recognized by the S-transceiver, zeros are looped back in the B and D-channels (DU) for four frames.

2.4.5 State Machine

The state diagram notation is given in **Figure 11**.

The information contained in the state diagrams are:

– state name
– Signal received from the line interface (INFO)
– Signal transmitted to the line interface (INFO)
– C/I code received (commands)
– C/I code transmitted (indications)
– transition criteria

The transition criteria are grouped into:

– C/I commands
– Signals received from the line interface (INFOs)
– Reset

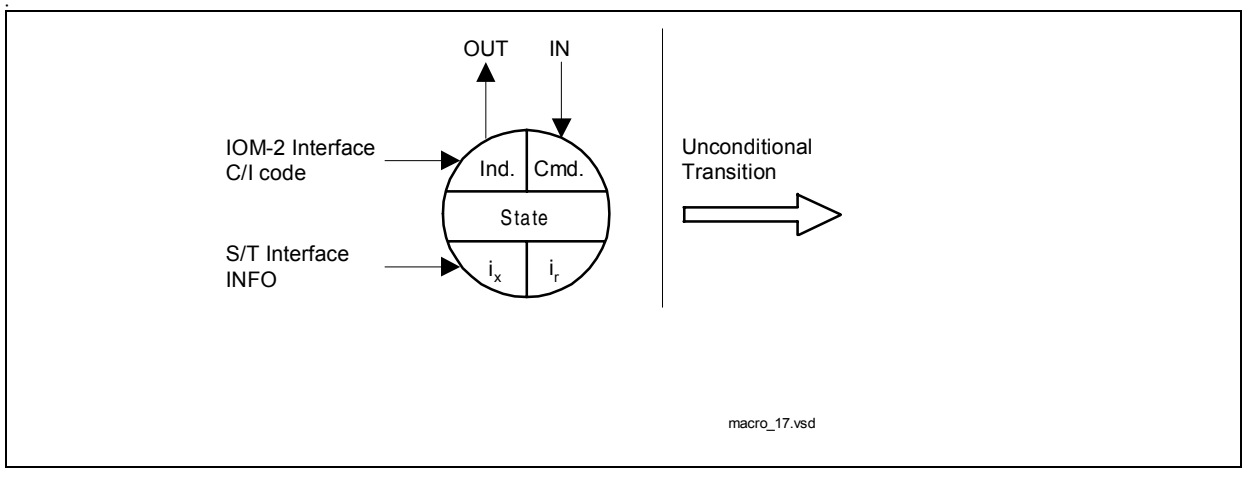


Figure 11 State Diagram Notation

As can be seen from the transition criteria, combinations of multiple conditions are possible as well. A “∗” stands for a logical AND combination. And a “+” indicates a logical OR combination.

Test Signals

- 2 kHz Single Pulses (TM1)

  One pulse with a width of one bit period per frame with alternating polarity.
- 96 kHz Continuous Pulses (TM2)

  Continuous pulses with a pulse width of one bit period.

Note: The test signals TM1 and TM2 can be generated via pins TM0-2 according to **Table 5**.

Reset States

After an active signal on the reset pin $\overline{\text{RST}}$ the S-transceiver state machine is in the reset state.

C/I Codes in Reset State

In the reset state the C/I code 0000 (TIM) is issued. This state is entered after a hardware reset ($\overline{\text{RST}}$).

C/I Codes in Deactivated State

If the S-transceiver is in state ‘Deactivated‘ and receives $\overline{\text{i0}}$, the C/I code 0000 (TIM) is issued until expiration of the 8 ms timer. Otherwise, the C/I code 1111 (DI) is issued.

Receive Infos on S/T

I0 INFO 0 detected

$\overline{I0}$	Level detected (signal different to I0)
I3	INFO 3 detected
$\overline{I3}$	Any INFO other than INFO 3

Transmit Infos on S/T

I0	INFO 0
I2	INFO 2
I4	INFO 4
It	Send Single Pulses (TM1). Send Continuous Pulses (TM2).

2.4.5.1 State Machine NT Mode

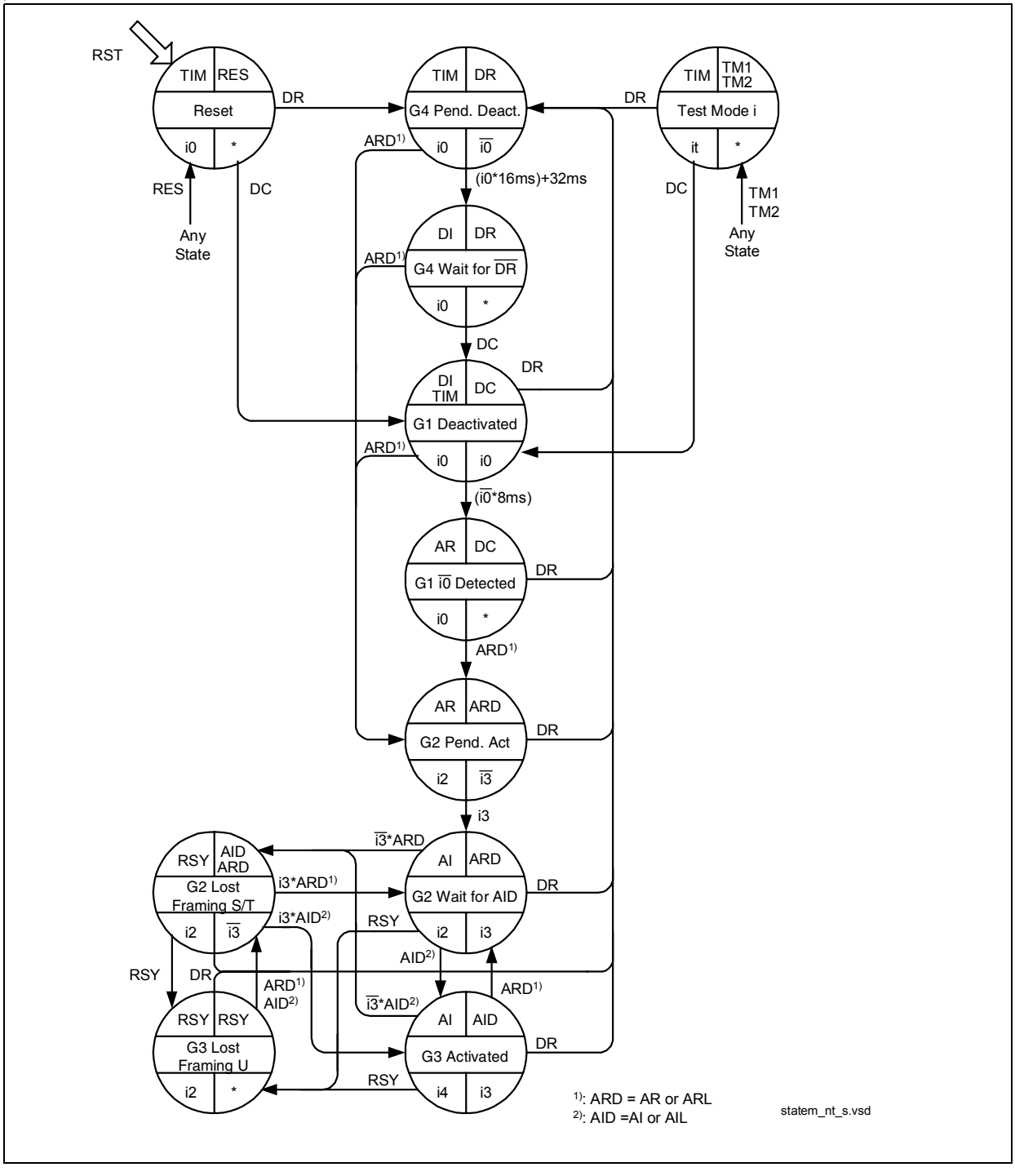


Figure 12 State Machine NT Mode

Note: By setting the Test Mode pins TM0-2 to ’010’ / ’011’: Continuous Pulses / Single Pulses, the S-transceiver starts sending the corresponding test signal, but no state transition is invoked.

G1 Deactivated

The S-transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. Activation is possible from the S/T interface and from the IOM®-2 interface.

G1 $\overline{\text{I0}}$ Detected

An $\overline{\text{INFO 0}}$ is detected on the S/T-interface, translated to an “Activation Request” indication in the C/I channel. The S-transceiver is waiting for an AR command, which normally indicates that the transmission line upstream is synchronized.

G2 Pending Activation

As a result of the ARD command, an INFO 2 is sent on the S/T-interface. INFO 3 is not yet received. In case of ARL command, loop 2 is closed.

G2 wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the S-transceiver waits for a “switch-through” command AID from the device upstream.

G3 Activated

INFO 4 is sent on the S/T-interface as a result of the “switch through” command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

G2 Lost Framing S/T

This state is reached when the transceiver has lost synchronism in the state G3 activated.

G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the transmission line, the S-transceiver transmits INFO 2.

G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state “G4 wait for DR”) is issued by the transceiver when:

either INFO0 is received for a duration of 16 ms

or an internal timer of 32 ms expires.

G4 wait for $\overline{\text{DR}}$

Final state after a deactivation request. The S-transceiver remains in this state until DC is issued.

Unconditional States

Test Mode TM1

Send Single Pulses

Test Mode TM2

Send Continuous Pulses

C/I Commands

Command	Abbr.	Code	Remark
Deactivation Request	DR	0000	Deactivation Request. Initiates a complete deactivation by transmitting INFO 0.
Reset	RES	0001	Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command.
Send Single Pulses	TM1	0010	Send Single Pulses.
Send Continuous Pulses	TM2	0011	Send Continuous Pulses.
Receiver not Synchronous	RSY	0100	Receiver is not synchronous
Activation Request	AR	1000	Activation Request. This command is used to start an activation.
Activation Request Loop	ARL	1010	Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface.
Activation Indication	AI	1100	Activation Indication. Synchronous receiver, i.e. activation completed.

Command	Abbr.	Code	Remark
Activation Indication Loop	AIL	1110	Activation Indication Loop
Deactivation Confirmation	DC	1111	Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

Indication	Abbr.	Code	Remark
Timing	TIM	0000	Interim indication during deactivation procedure.
Receiver not Synchronous	RSY	0100	Receiver is not synchronous.
Activation Request	AR	1000	$\overline{\text{INFO 0}}$ received from terminal. Activation proceeds.
Illegal Code Ciolation	CVR	1011	Illegal code violation received. This function has to be enabled in S_CONF0.EN_ICV.
Activation Indication	AI	1100	Synchronous receiver, i.e. activation completed.
Deactivation Indication	DI	1111	Timer (32 ms) expired or INFO 0 received for a duration of 16 ms after deactivation request.

3 Operational Description

3.1 Layer 1 Activation/Deactivation

3.1.1 Generation of 4B3T Signal Elements

For control and monitoring purposes of the activation/deactivation progress the following signal elements are defined by TS 102 080 and FTZ 1 TR 220.

Table 17 4B3T Signal Elements

U0	No signal or deactivation signal that is used in both directions. Downstream, it requests the NT to deactivate. Upstream, the NT acknowledges by U0 that it is deactivated.
U1W, U2W	Awake or awake acknowledge signal used in the awake procedure of the U-interface.
U2	The LT sends U2 to enable the own echo canceller to adapt the coefficients. By the Barker code the NT at the other end is enabled to synchronize. The detection of U2 is used by the NT as a criterion for synchronization. The M-channel on U may be used to transfer loop commands.
U2A	While the NT-RP is synchronizing on the received signal, the LT-RP sends out U2A to enable its echo canceller to adapt the coefficients, but sending no Barker code it inhibits the NT to synchronize on the still asynchronous signal. Due to proceeding synchronization, the U-frame may jump from time to time. U2A can not be detected in the NT at the far end.
U1A	U1A is similar to U1 but without framing information. While the NT synchronizes on the received signal, it sends out U1A to enable its echo canceller to adapt its coefficients, but sends no Barker code to prevent the LT from synchronizing on the still asynchronous signal. Due to proceeding synchronization, the U-frame may jump from time to time. U1A can not be detected by the far-end LT.
U1	When synchronized, the NT sends the Barker code and the LT may synchronize itself. U1 indicates additionally that a terminal equipment has not yet activated. Upon receiving U1 the LT indicates the synchronized state by C/I 'UAI' to layer-2. Usually during activation, no U1 signal is detected in the LT because the TE is activated first and U1 changes to U3 before being detected. The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.

Table 17 4B3T Signal Elements (cont'd)

U3	U3 indicates that the whole link to the TE is synchronous in both directions. On detecting U3 the LT requests the NT by U4H to establish a fully transparent connection. The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.
U4H	U4H requires the NT to go to the 'Transparent' state. On detecting U4H the NT stops sending signal U3 and informs the S-transceiver or a layer-2 device via the system interface. The M-channel on U may be used to transfer loop commands and 1 kbit/s transparent data.
U4	U4 transports operational data on B and D channels. The M-channel on U may be used to transfer loop commands and 1 kbit/s transparent data.
U5	U5 transports operational data on B and D channels. The M-channel on U may be used to transfer code error indications and 1 kbit/s transparent data.
SP	The T-SMINTO sends periodically single pulses once per millisecond on the U-interface. The test mode can be used for pulse mask measurements.
LOF	Loss of frame, generated by flywheel

Table 18 Generation of the 4B3T Signal Elements

Upstream (NT to LT)	Downstream (LT to NT)		symbols (ternary)	sync word (ternary)	M symbol (ternary)	binary data before scrambling
U1W	U2W	Resulting in a tone of: Frequency: 7.5 kHz Duration: 2.13 ms when sending the wakeup tone is finished, signal AWT is set and ternary "0" is sent	16 times + + + + + + + + – – – – – – – –	n/a	n/a	n/a
U1A	U2A	scrambled binary data		0	0	0
U1	U2	scrambled binary data		yes	yes	0
U3		scrambled binary data		yes	yes	1

Table 18 Generation of the 4B3T Signal Elements (cont'd)

	U4H	Duration: 1 ms (warranted by state machine)		yes	yes	1
U5	U4	Binary data from the digital interface		yes	yes	BBD
U0	U0	Ternary continuous "0"	0	0	0	n/a
SP	SP	single pulses	once "+", 119 times "0" (repeatedly)	n/a	n/a	n/a

Table 19 S/T-Interface Signals

Signals from NT to TE		**Signals from TE to NT**	
INFO 0	No signal.	INFO 0	No signal.
		INFO 1	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs.
INFO 2	Frame with all bits of B, D, and D-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.		
		INFO 3	Synchronized frames with operational data on B and D-channels.
INFO 4	Frames with operational data on B, D, and D-echo channels. Bit A set to binary ONE.		

3.1.2 Complete Activation Initiated by Exchange

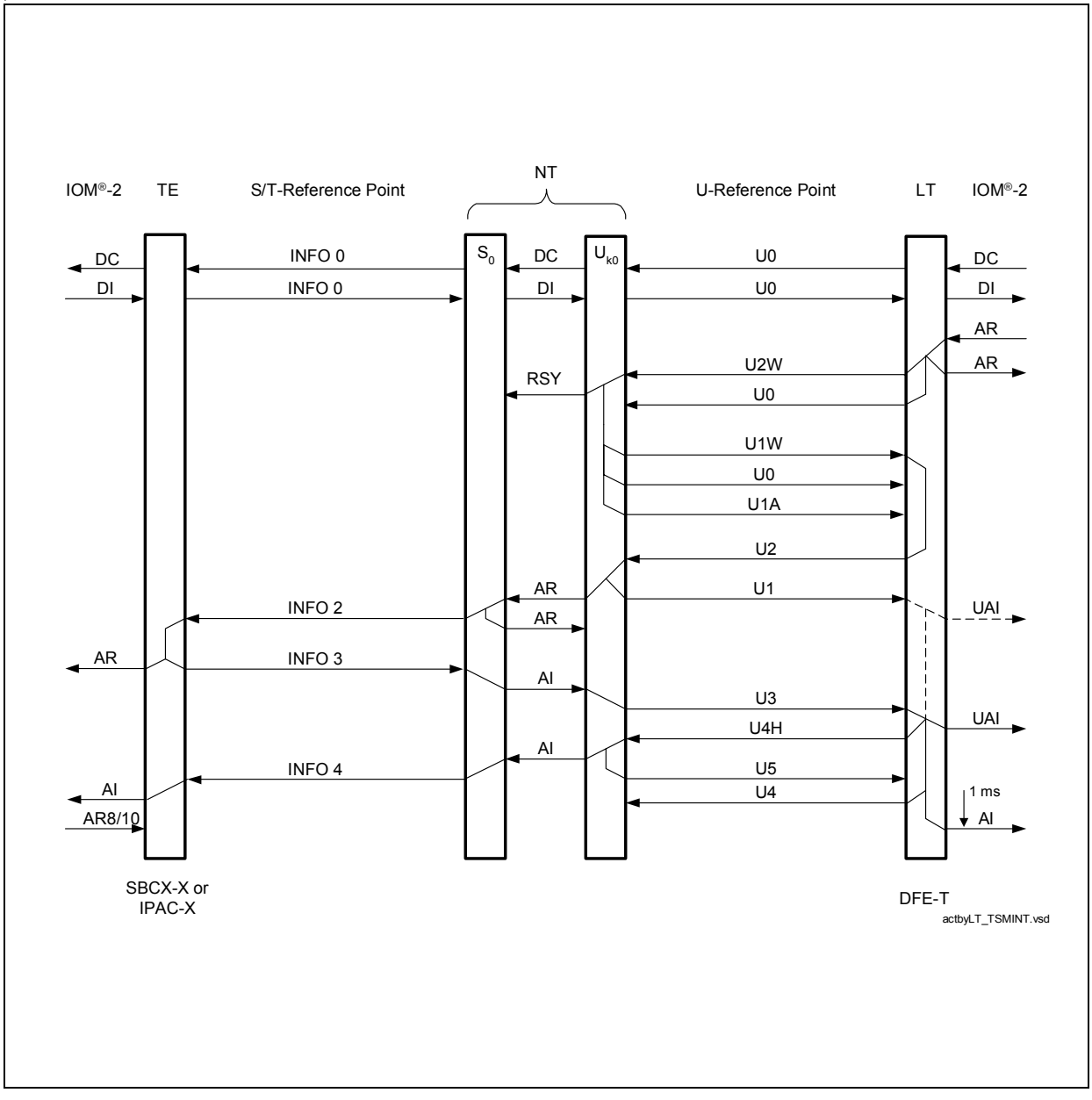


Figure 13 Activation Initiated by Exchange

Note: The LT starts issuing signal U2 before the NT starts issuing U1A. This chronological order is not displayed for clarification.

3.1.3 Complete Activation Initiated by TE

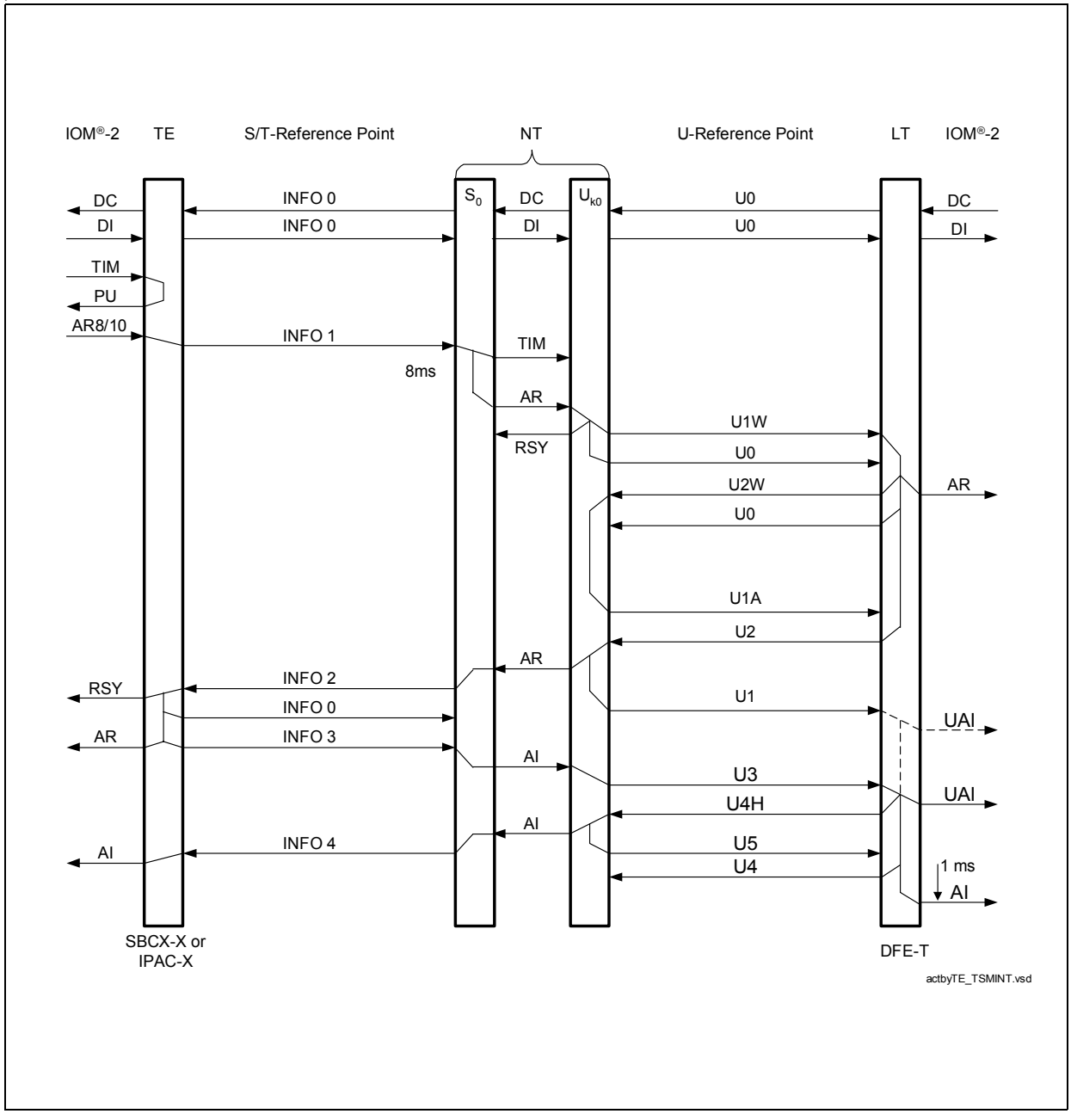


Figure 14 Activation Initiated by TE

Note: The LT starts issuing signal U2 before the NT starts issuing U1A. This chronological order is not displayed for clarification.

3.1.4 Deactivation

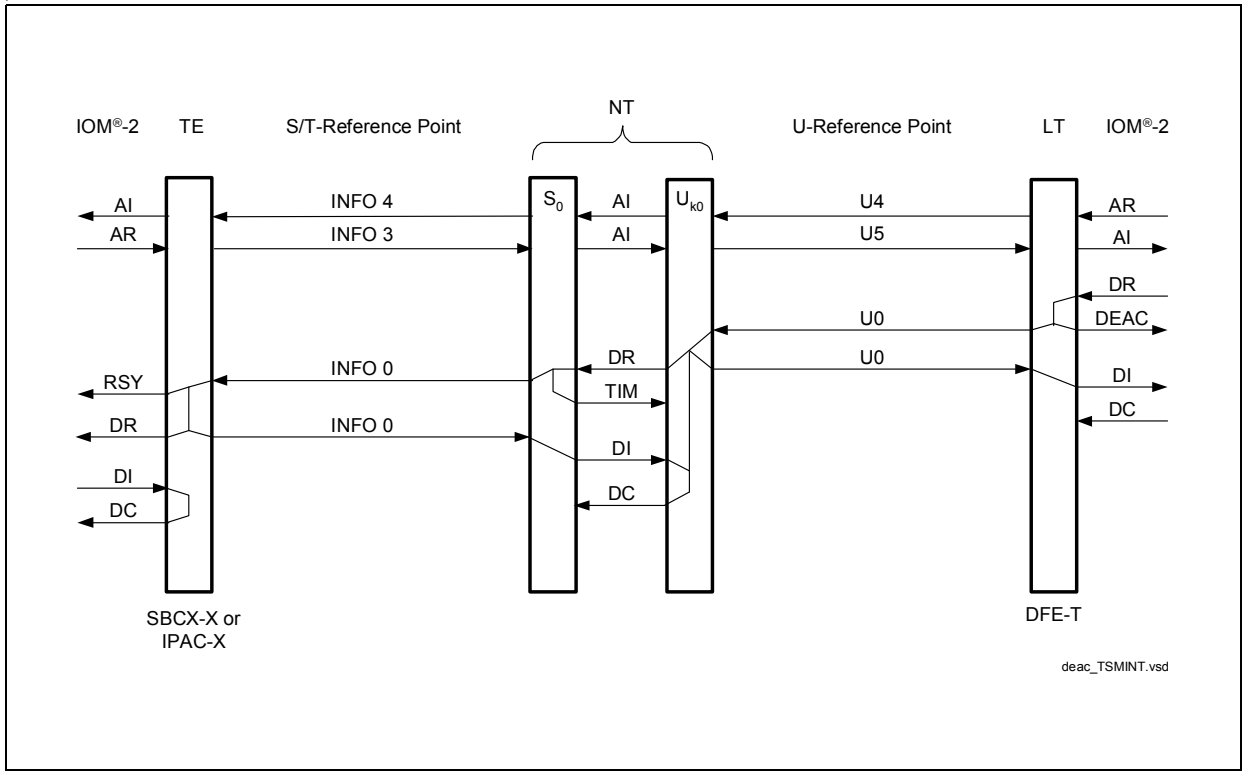


Figure 15 Deactivation (always Initiated by LT)

3.1.5 Activation Procedures with Loopback #2

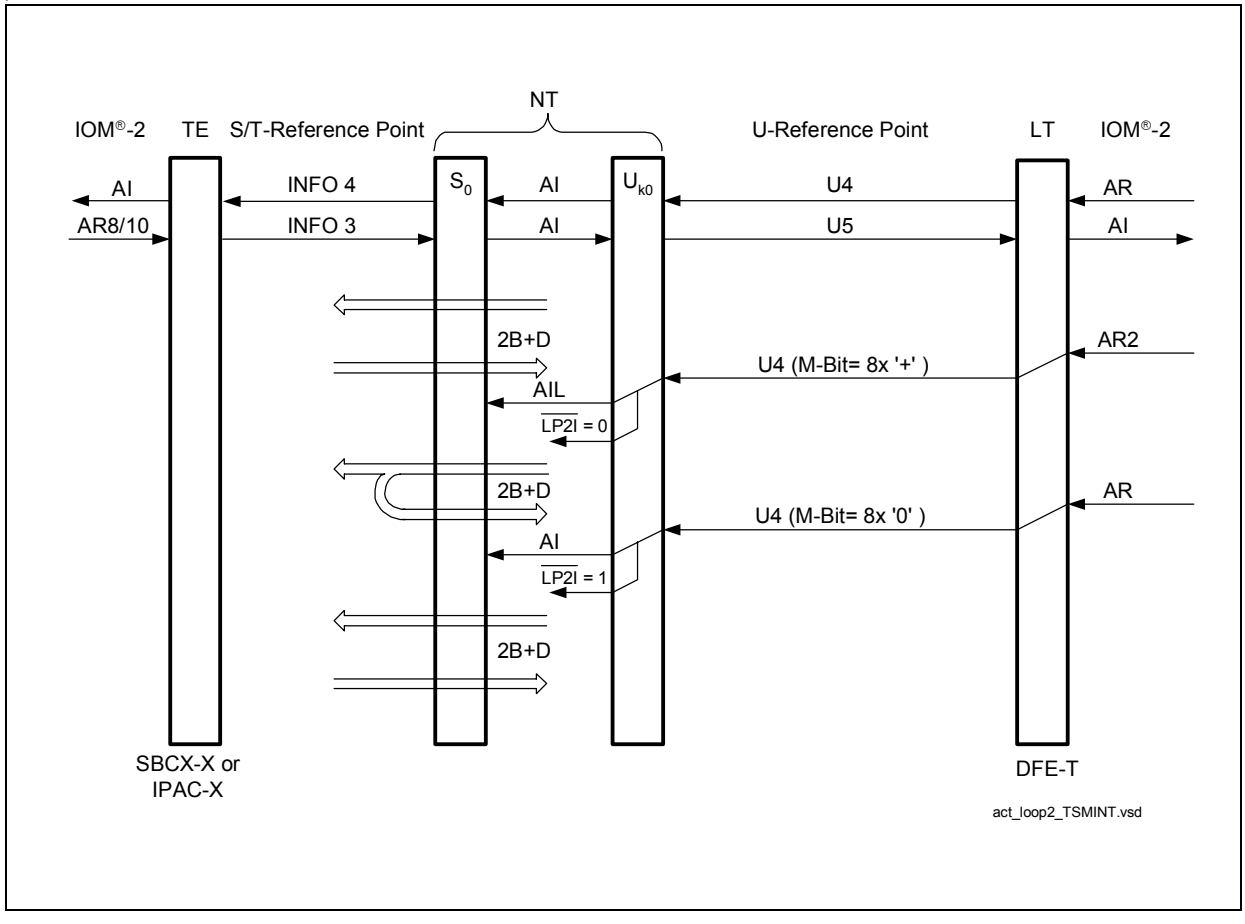


Figure 16 Activation of Loopback #2

Note: Closing/resolving loop 2 may provoke the S-transceiver to resynchronize. In this case, the following C/I-codes are exchanged immediately on reception of AIL/AI, respectively: DU: ’RSY’, DU: ’AI’, DD: ’AIL’/’AI’.

3.2 Layer 1 Loopbacks

Test loopbacks are specified by the national PTTs in order to facilitate the location of defect systems. Four different loopbacks are defined. The position of each loopback is illustrated in **Figure 17**.

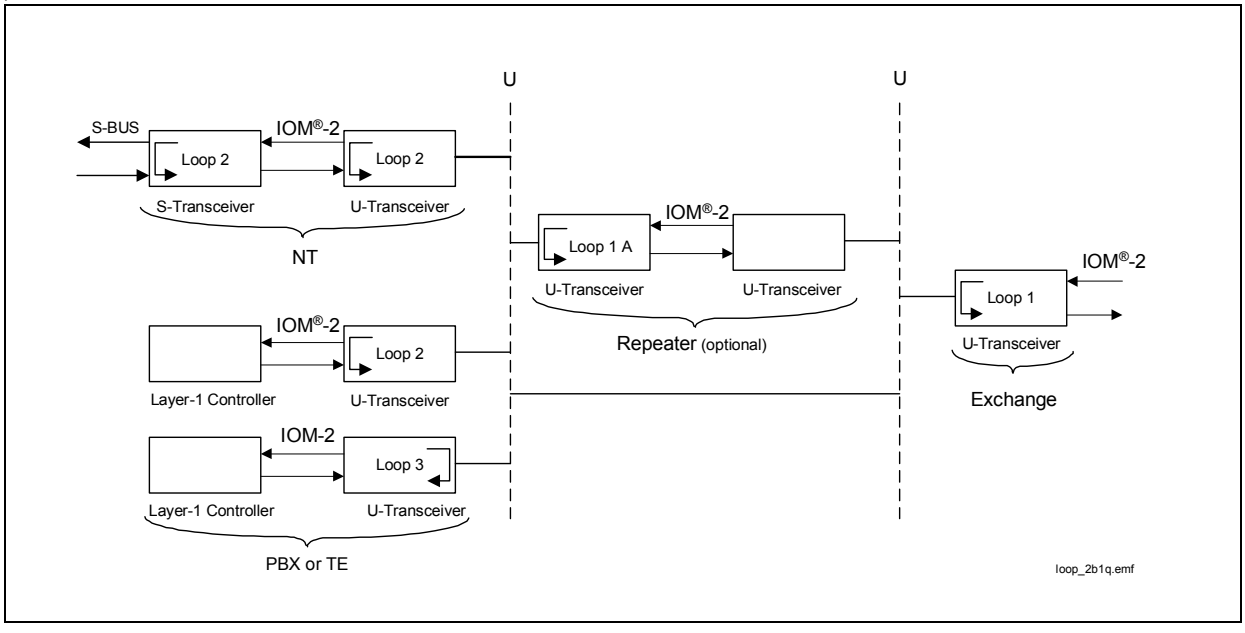


Figure 17 Test Loopbacks

Loopbacks #1, #1A and #2 are controlled by the exchange. Loopback #3 is controlled locally on the remote side. All four loopback types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner. Only the data looped back internally is processed; signals on the receive pins are ignored. The propagation delay of actually looped B and D channels data must be identical in all loopbacks.

3.2.1 Loopback No.2

The following loopback type belongs to the loopback-#2 category:

- complete loopback (B1,B2,D), in a downstream device

Normally loopback #2 is controlled by the exchange. The maintenance channel is used for this purpose.

3.2.1.1 Complete Loopback

When receiving the request for a complete loopback, the U transceiver passes it on to the S-bus transceiver. This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent”

3.3 External Circuitry

3.3.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.

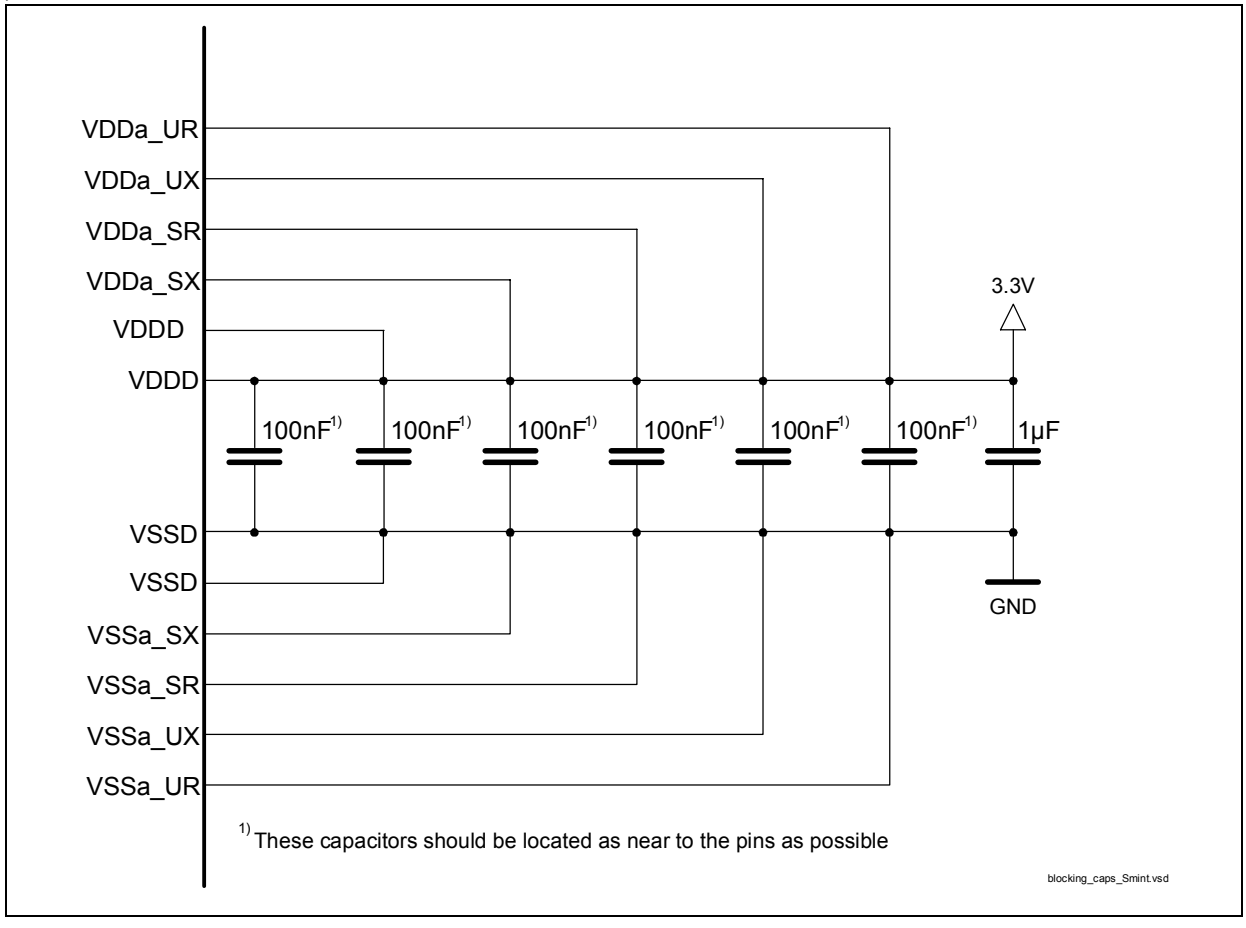


Figure 18 Power Supply Blocking

3.3.2 U-Transceiver

The T-SMINTO is connected to the twisted pair via a transformer. **Figure 19** shows the recommended external circuitry with external hybrid. The recommended protection circuitry is not displayed.

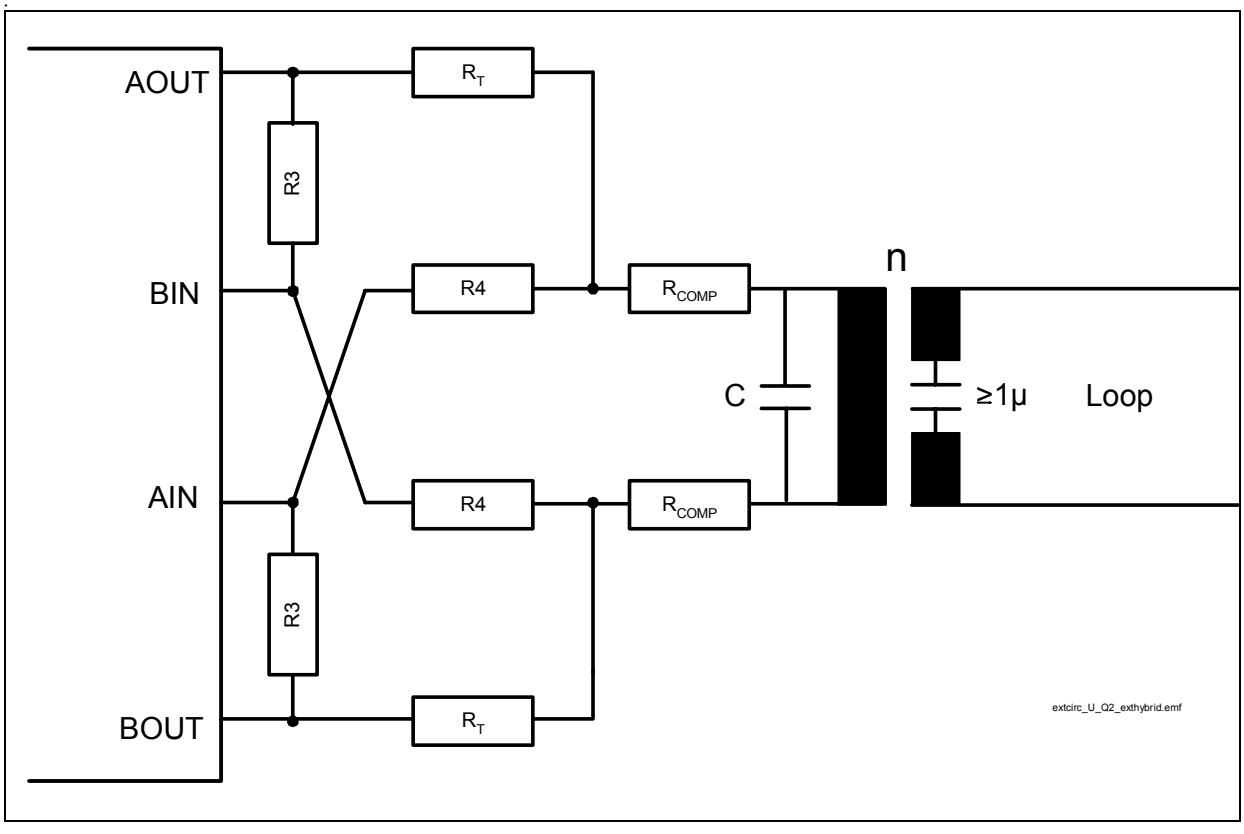


Figure 19 External Circuitry U-Transceiver with External Hybrid

U-Transformer Parameters

The following table lists parameters of typical U-transformers.

Table 20 U-Transformer Parameters

U-Transformer Parameters	Symbol	Value	Unit
U-Transformer ratio; Device side : Line side	n	1 : 1.6	
Main inductanc of windings on the line side	L_H	7.5	mH
Leakage inductance of windings on the line side	L_S	120	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	30	pF
DC resistance of the windings on device side	R_B	0.9	Ω
DC resistance of the windings on line side	R_L	1.8	Ω

Resistors of the External Hybrid R3, R4 and R_T

R3 = 1.75 kΩ

R4 = 1.0 kΩ

R_T = 25 Ω

Resistors R_{COMP} / R_T

- Optional use of trafos with non negligible resistance R_B, R_L requires compensation resistors R_{COMP} depending on R_B and R_L:

$$n^2 \times (2R_{COMP} + R_B) + R_L = 20\Omega \quad (1)$$

- Compliance with Return Loss Measurements:

$$n^2 \times (2R_{COMP} + 2R_T + R_{out} + R_B) + R_L = 150\Omega \quad (2)$$

R_B, R_L : see **Table 20**
R_{OUT} : see **Table 25**

15nF Capacitor

To achieve optimum performance the 15nF capacitor should be MKT. A Ceramic capacitor is not recommended.

Tolerances

- Rs: 1%
- C = 15nF: 10-20%
- L_H = 7.5mH: 10%

3.3.3 S-Transceiver

In order to comply to the physical requirements of ITU recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the S-transceiver needs some additional circuitry.

S-Transformer Parameters

The following **Table 21** lists parameters of a typical S-transformer:

Table 21 S-Transformer Parameters

Transformer Parameters	Symbol	Value	Unit
Transformer ratio; Device side : Line side	n	2 : 1	
Main inductance of windings on the line side	L_H	typ. 30	mH
Leakage inductance of windings on the line side	L_S	typ. <3	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	typ. <100	pF
DC resistance of the windings on device side	R_B	typ. 2.4	Ω
DC resistance of the windings on line side	R_L	typ. 1.4	Ω

Transmitter

The **transmitter** requires external resistors R_{stx} = 47Ω in order to adjust the output voltage to the pulse mask (nominal 750 mV according to ITU I.430, to be tested with the test mode “TM1”) on the one hand and in order to meet the output impedance of minimum 20 Ω on the other hand (to be tested with the testmode ’Continuous Pulses’) on the other hand.

Note: The resistance of the S-transformer must be taken into account when dimensioning the external resistors R_{stx}. If the transmit path contains additional components (e.g. a choke), then the resistance of these additional components must be taken into account, too.

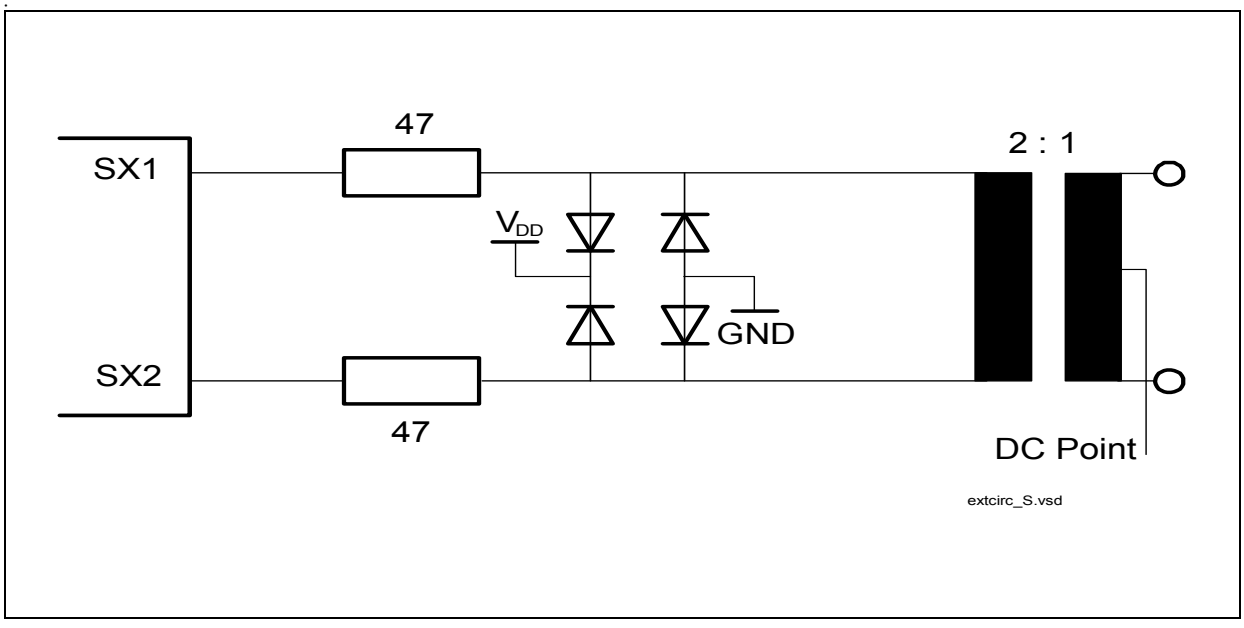


Figure 20 External Circuitry S-Interface Transmitter

Receiver

The **receiver** of the S-transceiver is symmetrical. 10 kΩ overall resistance are recommended in each receive path. It is preferable to split the resistance into two resistors for each line. This allows to place a high resistance between the transformer and the diode protection circuit (required to pass 96 kHz input impedance test of ITU I.430 [6] and ETS 300012-1). The remaining resistance (1.8 kΩ) protects the S-transceiver itself from input current peaks.

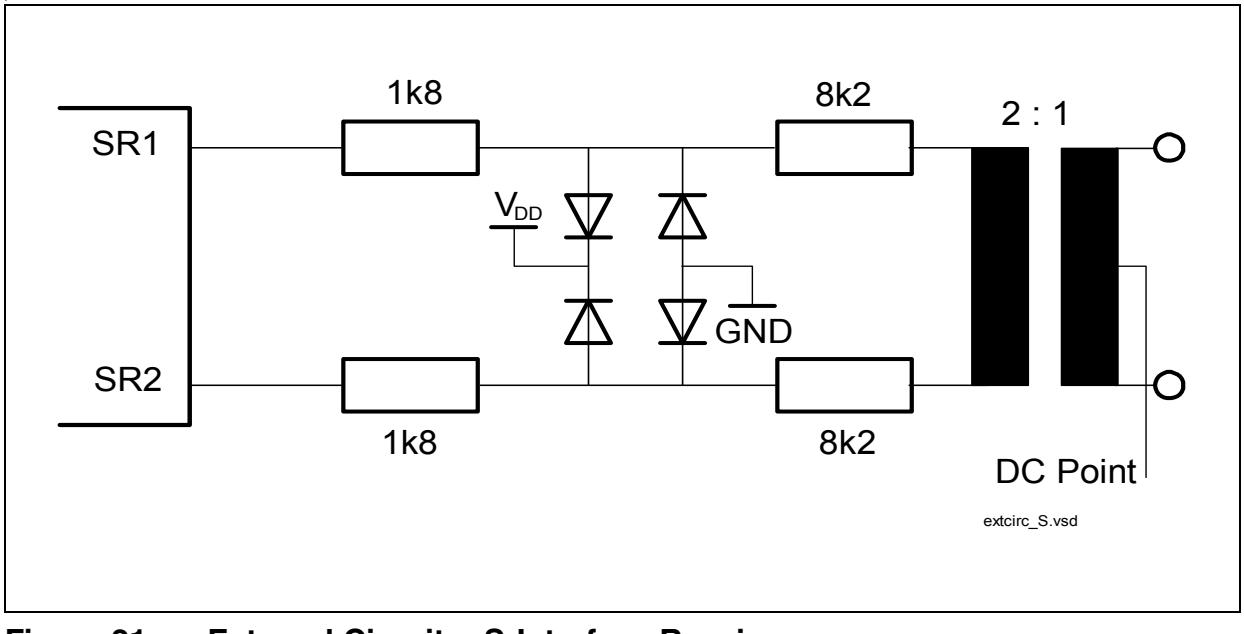


Figure 21 External Circuitry S-Interface Receiver

3.3.4 Oscillator Circuitry

Figure 22 illustrates the recommended oscillator circuit.

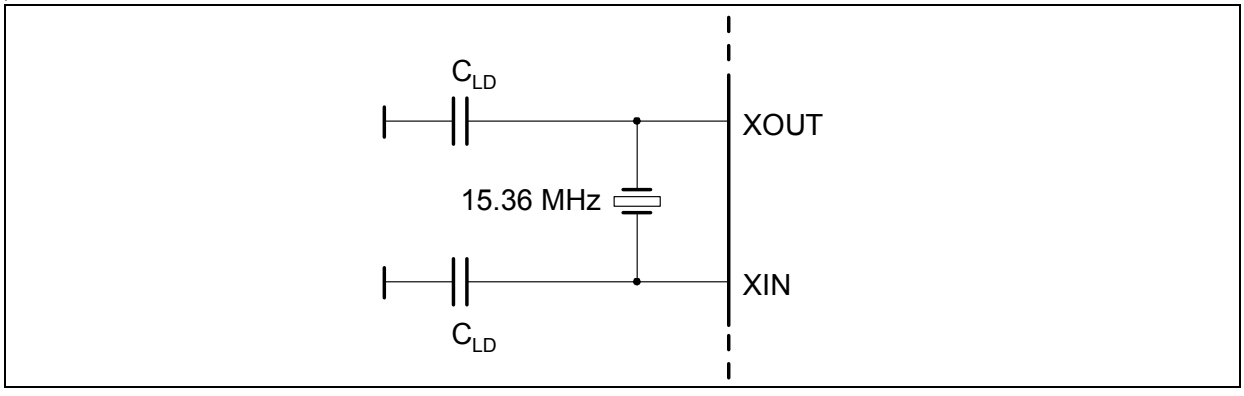


Figure 22 Crystal Oscillator

Table 22 Crystal Parameters

Parameter	Symbol	Limit Values	Unit
Frequency	f	15.36	MHz
Frequency calibration tolerance		+/-60	ppm
Load capacitance	C_L	20	pF
Max. resonance resistance	R1	20	Ω
Max. shunt capacitance	C_0	7	pF
Oscillator mode		fundamental	

External Components and Parasitics

The load capacitance C_L is computed from the external capacitances C_{LD}, the parasitic capacitances C_{Par} (pin and PCB capacitances to ground and V_{DD}) and the stray capacitance C_{IO} between XIN and XOUT:

$$C_L = \frac{(C_{LD} + C_{Par}) \times (C_{LD} + C_{Par})}{(C_{LD} + C_{Par}) + (C_{LD} + C_{Par})} + C_{IO}$$

For a specific crystal the total load capacitance is predefined, so the equation must be solved for the external capacitances C_{LD}, which is usually the only variable to be determined by the circuit designer. Typical values for the capacitances C_{LD} connected to the crystal are 22 - 33 pF.

3.3.5 General

– low power LEDs

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	-40 to 85	°C
Storage temperature	T_{STG}	– 65 to 150	°C
Maximum Voltage on V_{DD}	V_{DD}	4.2	V
Maximum Voltage on any pin with respect to ground	V_S	-0.3 to V_{DD} + 3.3 (max. < 5.5)	V

ESD integrity (according EIA/JESD22-A114B (HBM)): 2 kV

Note: Stress above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Line Overload Protection

The T-SMINT®O is compliant to ESD tests according to ANSI / EOS / ESD-S 5.1-1993 (CDM), EIA/JESD22-A114B (HBM) and to Latch-up tests according to JEDEC EIA / JESD78. From these tests the following max. input currents are derived (**Table 23**):

Table 23 Maximum Input Currents

Test	Pulse Width	Current	Remarks
ESD	100 ns	1.3 A	3 repetitions
Latch-up	5 ms	+/-200 mA	2 repetitions, respectively
DC	--	10 mA	

4.2 DC Characteristics

.

V_{DD}/V_{DDA} = 3.3 V +/- 5% ; V_{SS}/V_{SSA} = 0 V; T_A = -40 to 85 °C

Digital Pins	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
All	Input low voltage	V_{IL}	-0.3	0.8	V	
	Input high voltage	V_{IH}	2.0	5.25	V	
All except DD/DU $\overline{ACT}$,$\overline{LP2I}$ MCLK	Output low voltage	V_{OL1}		0.45	V	I_{OL1} = 3.0 mA
	Output high voltage	V_{OH1}	2.4		V	I_{OH1} = 3.0 mA
DD/DU $\overline{ACT}$,$\overline{LP2I}$ MCLK	Output low voltage	V_{OL2}		0.45	V	I_{OL2} = 4.0 mA
	Output high voltage (DD/DU push-pull)	V_{OH2}	2.4		V	I_{OH2} = 4.0 mA
All	Input leakage current	I_{LI}		10	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Output leakage current	I_{LO}		10	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Input leakage current (internal pull-up)	I_{LIPU}	50	200	µA	0 V ≤ V_{IN} ≤ V_{DD}
Analog Pins						
AIN, BIN	Input leakage current	I_{LI}		30	µA	0 V ≤ V_{IN} ≤ V_{DD}

Table 24 S-Transceiver Characteristics

Pin	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
SX1,2	Absolute value of output pulse amplitude (V_{SX2} - V_{SX1})	V_X	2.03	2.2	2.31	V	R_L = 50 Ω
SX1,2	S-Transmitter output impedance	Z_X	10	34		kΩ	see [1]
			0				see [2][3]
SR1,2	S-Receiver input impedance	Z_R	10 100			kΩ Ω	V_{DD} = 3.3 V V_{DD} = 0 V

1) Requirement ITU-T I.430, chapter 8.5.1.1a): 'At all times except when transmitting a binary zero, the output impedance , in the frequency range of 2kHz to 1 MHz, shall exceed the impedance indicated by the template in Figure 11. The requirement is applicable with an applied sinusoidal voltage of 100 mV (r.m.s value)'

2) Requirement ITU-T I.430, chapter 8.5.1.1b): 'When transmitting a binary zero, the output impedance shall be > 20 Ω.': Must be met by external circuitry.

3) Requirement ITU-T I.430, chapter 8.5.1.1b), Note: 'The output impedance limit shall apply for a nominal load impedance (resistive) of 50 Ω. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value +/- 10%. The peak amplitude shall be defined as the the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.'

Table 25 U-Transceiver Characteristics

	Limit Values			Unit
	min.	typ.	max.	
Receive Path				
Signal / (noise + total harmonic distortion)[1]	65[2]			dB
DC-level at AD-output	45	50	55	%[3]
Threshold of level detect (measured between AIN and BIN with respect to zero signal)	10		23	mV peak
Input impedance AIN/BIN	80			kΩ
Transmit Path				
Signal / (noise + total harmonic distortion)[4]	70			dB
Common mode DC-level	1.61	1.65	1.69	V
Offset between AOUT and BOUT			35	mV
Absolute peak voltage for a single +3 or -3 pulse measured between AOUT and BOUT[5]	2.42	2.5	2.58	V
Output impedance AOUT/BOUT: Power-up Power-down		 0.8 3	 1.5 6	 Ω Ω

1) Test conditions: 1.4 Vpp differential sine wave as input on AIN/BIN with long range (low, critical range).

2) Versions PEF 8x913 with enhanced performance of the U-interface are tested with tightened limit values

3) The percentage of the "1 "-values in the PDM-signal.

4) Interpretation and test conditions: The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 70 dB below the signal for an evenly distributed but otherwise random sequence of +3, +1, -1, -3.

5) The signal amplitude measured over a period of 1 min. varies less than 1%.

4.3 Capacitances

T_A = 25 °C, 3.3 V ± 5 % V_{SSA} = 0 V, V_{SSD} = 0 V, f_c = 1 MHz, unmeasured pins grounded.

Table 26 Pin Capacitances

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Digital pads: Input Capacitance I/O Capacitance	 C_{IN} $C_{I/O}$		 7 7	 pF pF	
Analog pads: Load Capacitance	 C_L		 3	 pF	 pin AIN, BIN

4.4 Power Consumption

Power Consumption

VDD=3.3 V, VSS=0 V, Inputs at VSS/VDD, no LED connected, 50% bin. zeros, no output loads except SX1,2 (50 Ω[1)])

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
Operational U and S enabled, IOM®-2 off		 185 165		 mW mW	 U: ETSI loop 1 (0 m) U: ETSI Loop 2 (typical line)
Power Down		15		mW	

1) 50 Ω (2 x TR) on the S-bus.

4.5 Supply Voltages

VDD_D = + Vdd ± 5%
VDD_A = + Vdd ± 5%

The maximum sinusoidal ripple on VDD is specified in the following figure:

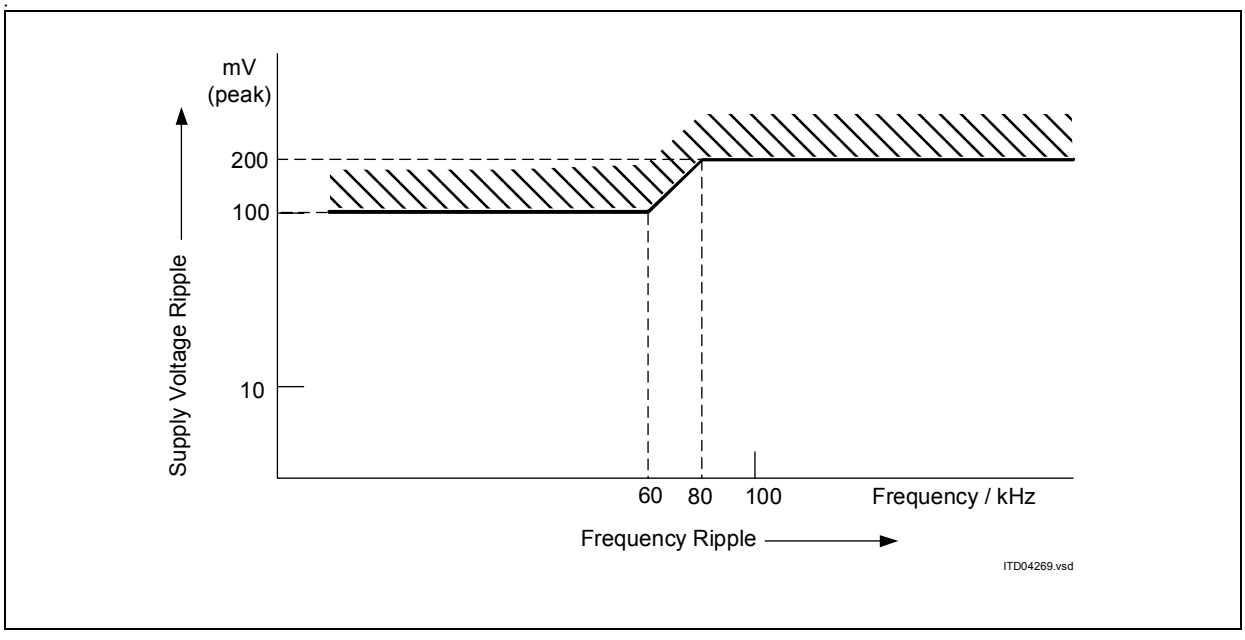


Figure 23 Maximum Sinusoidal Ripple on Supply Voltage

4.6 AC Characteristics

T_A = -40 to 85 °C, V_{DD} = 3.3 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **Figure 24**.

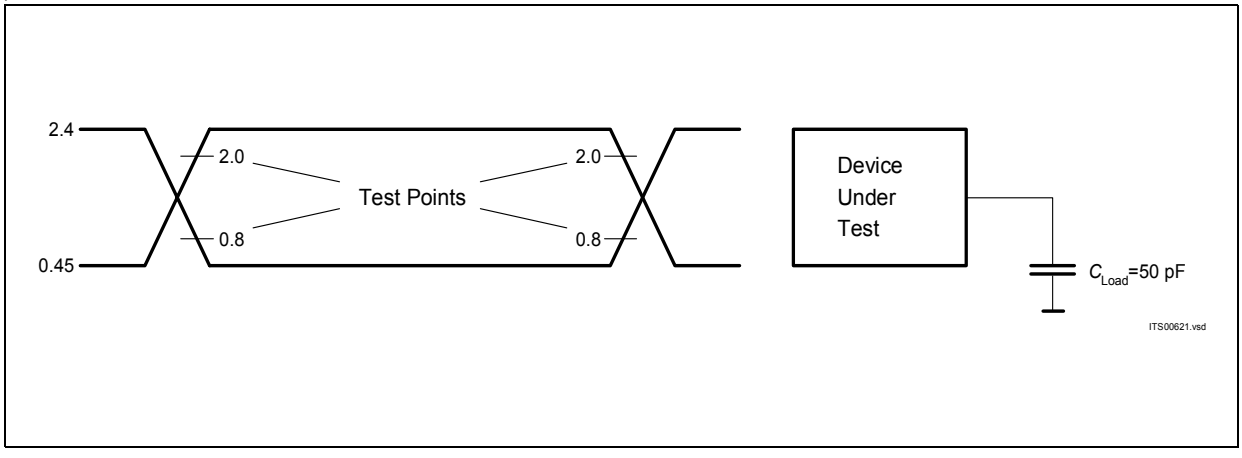


Figure 24 Input/Output Waveform for AC Tests

Parameter All Output Pins	Symbol	Limit values		Unit
		Min	Max	
Fall time			30	ns
Rise time			30	ns

4.6.1 IOM-2 Interface

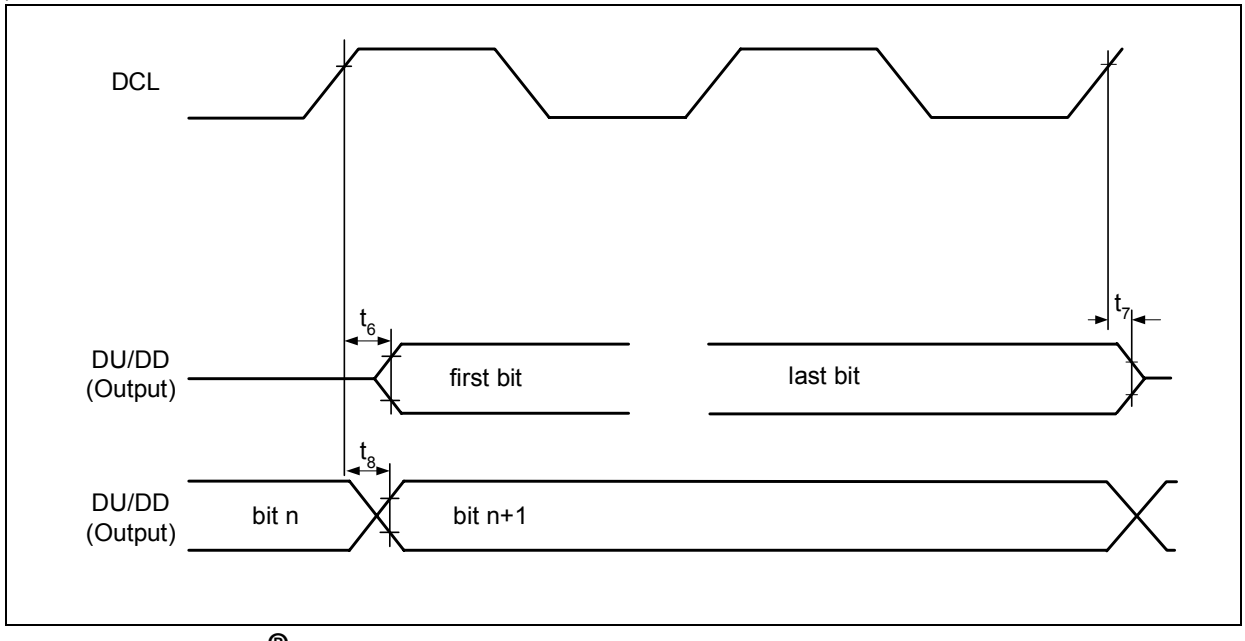


Figure 25 IOM®-2 Interface - Bit Synchronization Timing

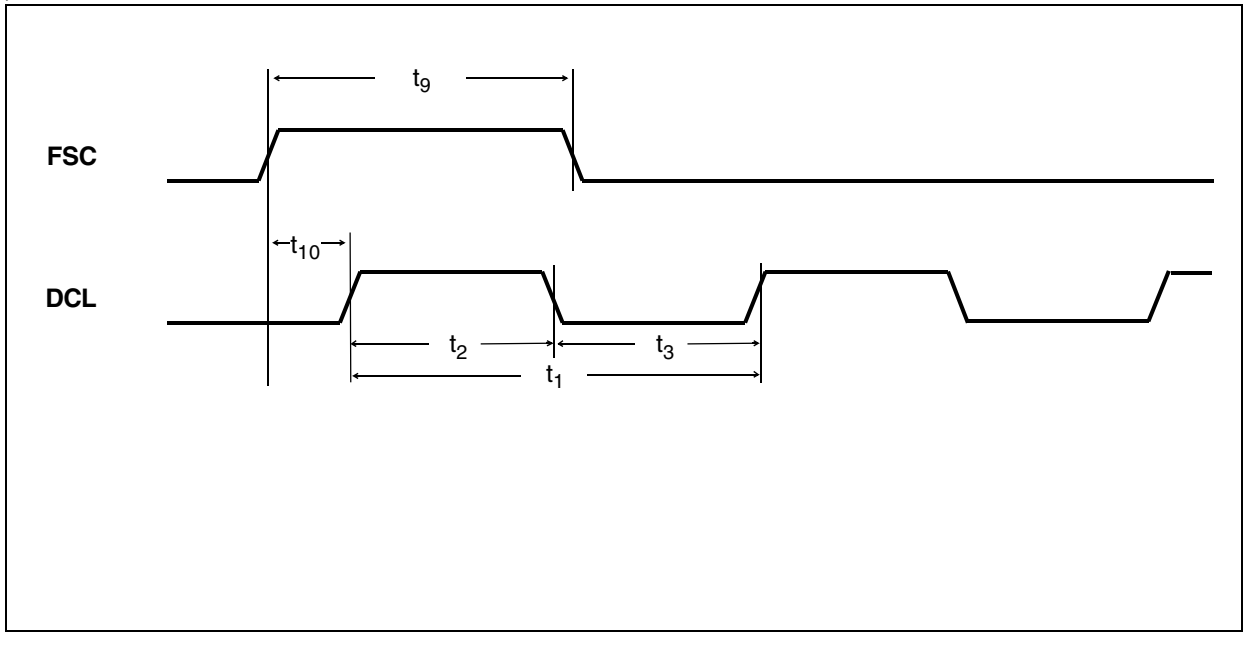


Figure 26 IOM-2 Interface - Frame Synchronization Timing

Note: At the start and end of a reset period, a frame jump may occur. This results in a DCL and FSC high time of min. 130 ns after this specific event.

Parameter IOM®-2 Interface	Symbol	Limit values			Unit
		Min	Typ	Max	
DCL period	t_1	1875	1953	2035	ns
DCL high	t_2	850	960	1105	ns
DCL low	t_3	850	960	1105	ns
Output data from high impedance to active (FSC high or other than first timeslot)	t_6			100	ns
Output data from active to high impedance	t_7			100	ns
Output data delay from clock	t_8			80	ns
FSC high	t_9		50% of FSC cycle time		ns
FSC advance to DCL	t_{10}	65	130	195	ns
DCL, FSC rise/fall	t_{15}			30	ns
Data out rise/fall (C_L = 50 pF, tristate)	t_{17}			150	ns

4.6.2 Reset

Table 27 Reset Input Signal Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Length of active low state	$t_{\overline{RST}}$	4			ms	Power On the 4 ms are assumed to be long enough for the oscillator to run correctly
		2 x DCL clock cycles + 400 ns				After Power On

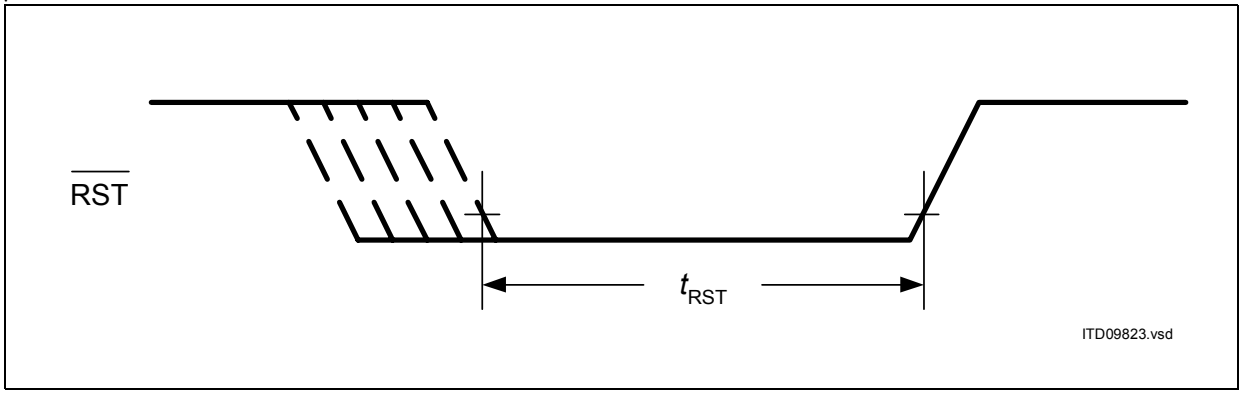


Figure 27 Reset Input Signal

4.6.3 Undervoltage Detection Characteristics

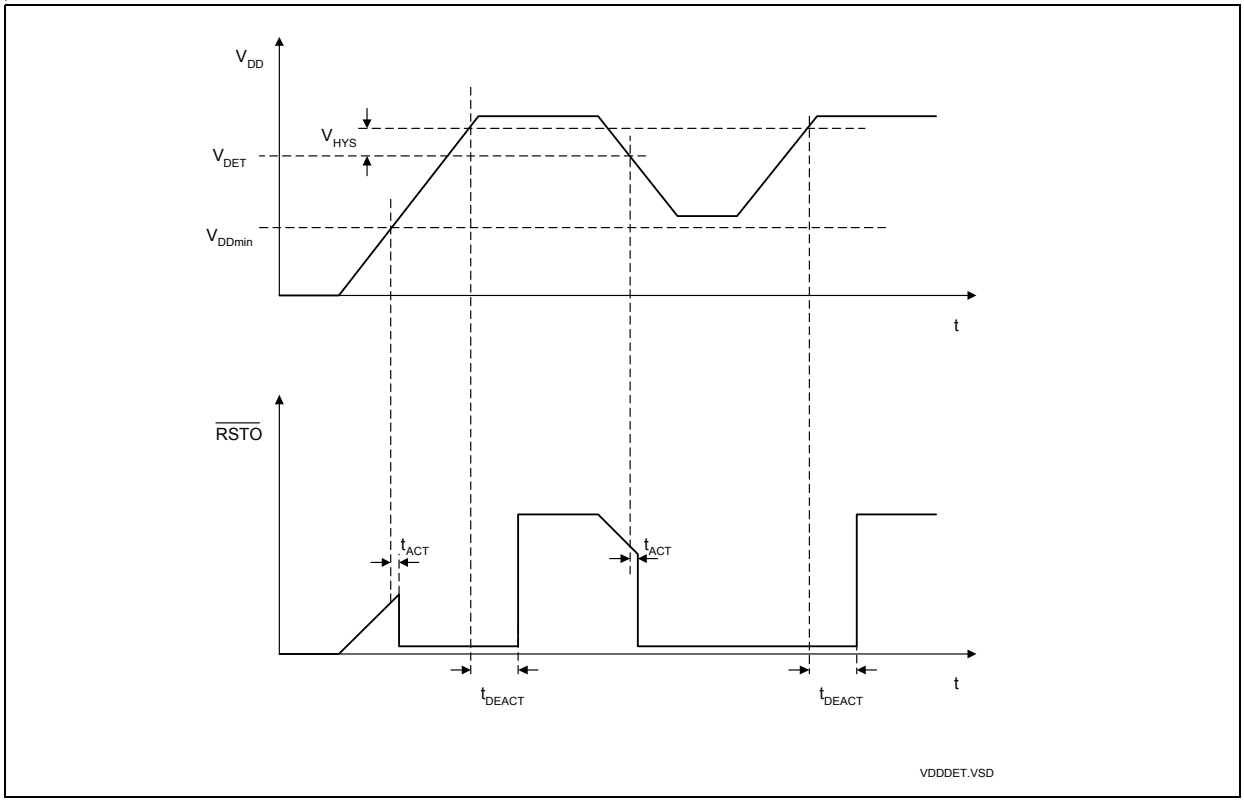


Figure 28 Undervoltage Control Timing

Table 28 Parameters of the UVD/POR Circuit

V_{DD}= 3.3 V ± 5 %; V_{SS}= 0 V; T_A = -40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Detection Threshold[1)]	V_{DET}	2.7	2.8	2.92	V	V_{DD} = 3.3 V ± 5 %
Hysteresis	V_{Hys}	30		90	mV	
Max. rising/falling V_{DD} edge for activation/ deactivation of UVD	dV_{DD}/dt			0.1	V/µs	
Max. rising V_{DD} for power-on[2)]				0.1	V/ ms	
Min. operating voltage	V_{DDmin}	1.5			V	

V_{DD}= 3.3 V ± 5 %; V_{SS}= 0 V; T_A = -40 to 85 °C

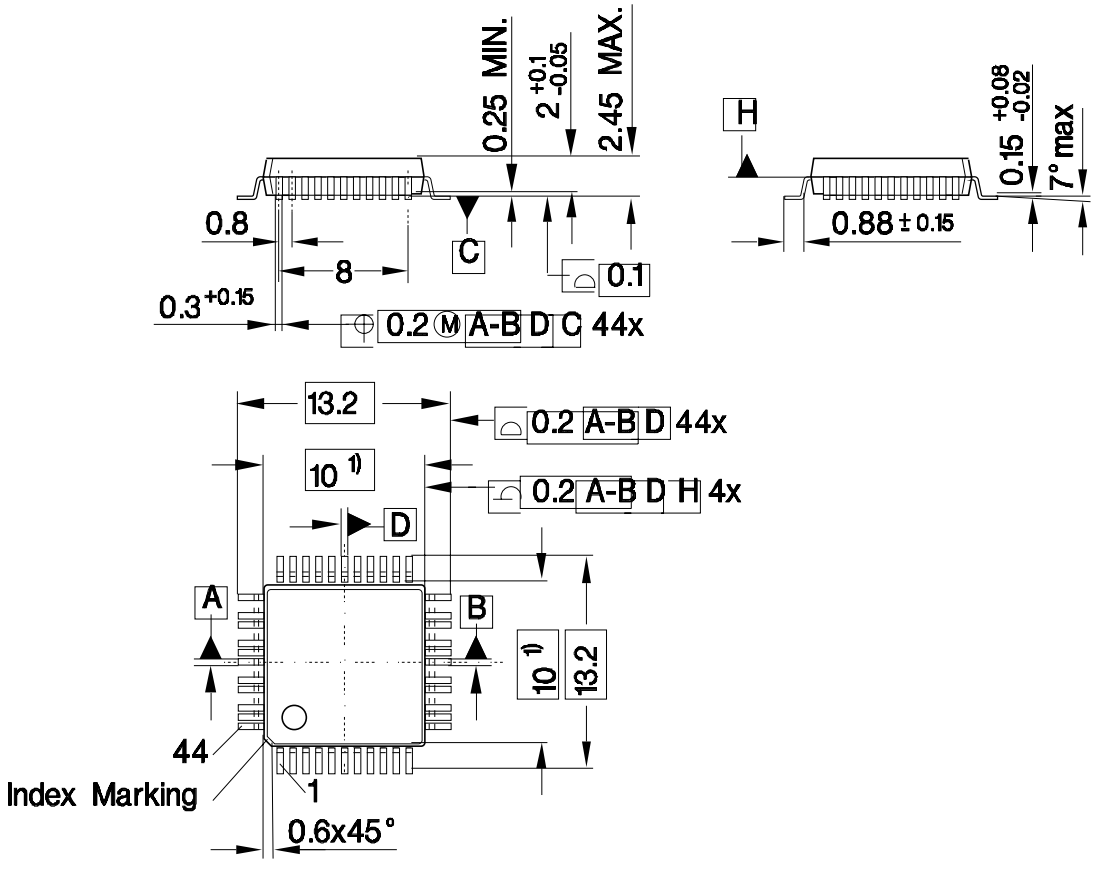
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Delay for activation of $\overline{\text{RSTO}}$	t_{ACT}			10	µs	
Delay for deactivation of $\overline{\text{RSTO}}$	t_{DEACT}		64		ms	

1) The Detection Threshold V_{DET} is far below the specified supply voltage range of analog and digital parts of the T-SMINT®. Therefore, the board designer must take into account that a range of voltages is existing, where neither performance and functionality of the T-SMINT® are guaranteed, nor a reset is generated.

2) If the integrated Power-On Reset of the T-SMINTO is selected ($\overline{\text{VDDDET}}$ = '0') and the supply voltage V_{DD} is ramped up from 0V to 3.3V +/- 5%, then the T-SMINTO is kept in reset during $V_{DDmin} < V_{DD} < V_{DET} + V_{Hys}$. V_{DD} must be ramped up so slowly that the T-SMINTO leaves the reset state after the oscillator circuit has already finished start-up. The start-up time of the oscillator circuit is typically in the range between 3ms and 12ms.

5 Package Outlines

Plastic Package, P-MQFP-44
(Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

6 Appendix: Differences between Q- and T-SMINT®O

The Q- and T-SMINT®O have been designed to be as compatible as possible. However, some differences between them are unavoidable due to the different line codes 2B1Q and 4B3T used for data transmission on the U_{k0} line.

Especially the pin compatibility between Q- and T-SMINT®O allows for one single PCB design for both series with only some mounting differences.

The following chapter summarizes the main differences between the Q- and T-SMINT®O.

6.1 Pinning

6.1.1 Pin Definitions and Functions

Table 29 Pin Definitions and Functions

Pin MQFP-44		Q-SMINT®O: 2B1Q	T-SMINT®O: 4B3T
10		Triple-Last-Look ($\overline{TLL}$)	Tie to ‘1‘
11		Metallic Termination Input (MTI)	Tie to ‘1‘
16		Auto U Activation (AUA)	Tie to ‘1‘
17		Cold Start Only (CSO)	Tie to ‘1‘
38		Power Status (primary) (PS1)	Tie to ‘1‘
26		Power Status (secondary) (PS2)	Tie to ‘1‘

6.1.2 LED Pin $\overline{ACT}$

The 4 LED states (off, fast flashing, slow flashing, on), which can be displayed with pin $\overline{ACT}$, are slightly different for Q- and T-SMINT®O (see **Table 30**).

Table 30 $\overline{ACT}$ States

LED States	Pin $\overline{ACT}$	
	Q-SMINT®O: 2B1Q	T-SMINT®O: 4B3T
off	V_{DD}	V_{DD}
fast flashing	8Hz (1 : 1)*	2Hz (1 : 1)*

Table 30 $\overline{\text{ACT}}$ States (cont'd)

LED States	Pin $\overline{\text{ACT}}$	
	Q-SMINT®O: 2B1Q	**T-SMINT®O: 4B3T**
slow flashing	1Hz (1 : 1)*	1Hz (3 : 1)*
on	GND	GND

Note: * denotes the duty cycle 'high' : 'low'.

6.2 U-Transceiver

6.2.1 U-Interface Conformity

Table 31 Related Documents to the U-Interface

	Q-SMINT®O: 2B1Q	**T-SMINT®O: 4B3T**
ETSI: TS 102 080	conform to annex A compliant to 10 ms interruptions	conform to annex B
ANSI: T1.601-1998 (Revision of ANSI T1.601-1992)	conform MLT input and decode logic	not required
CNET: ST/LAA/ELR/DNP/822	conform	not required
RC7355E	conform	not required
FTZ-Richtlinie 1 TR 220	not required	conform

6.2.2 U-Transceiver State Machines

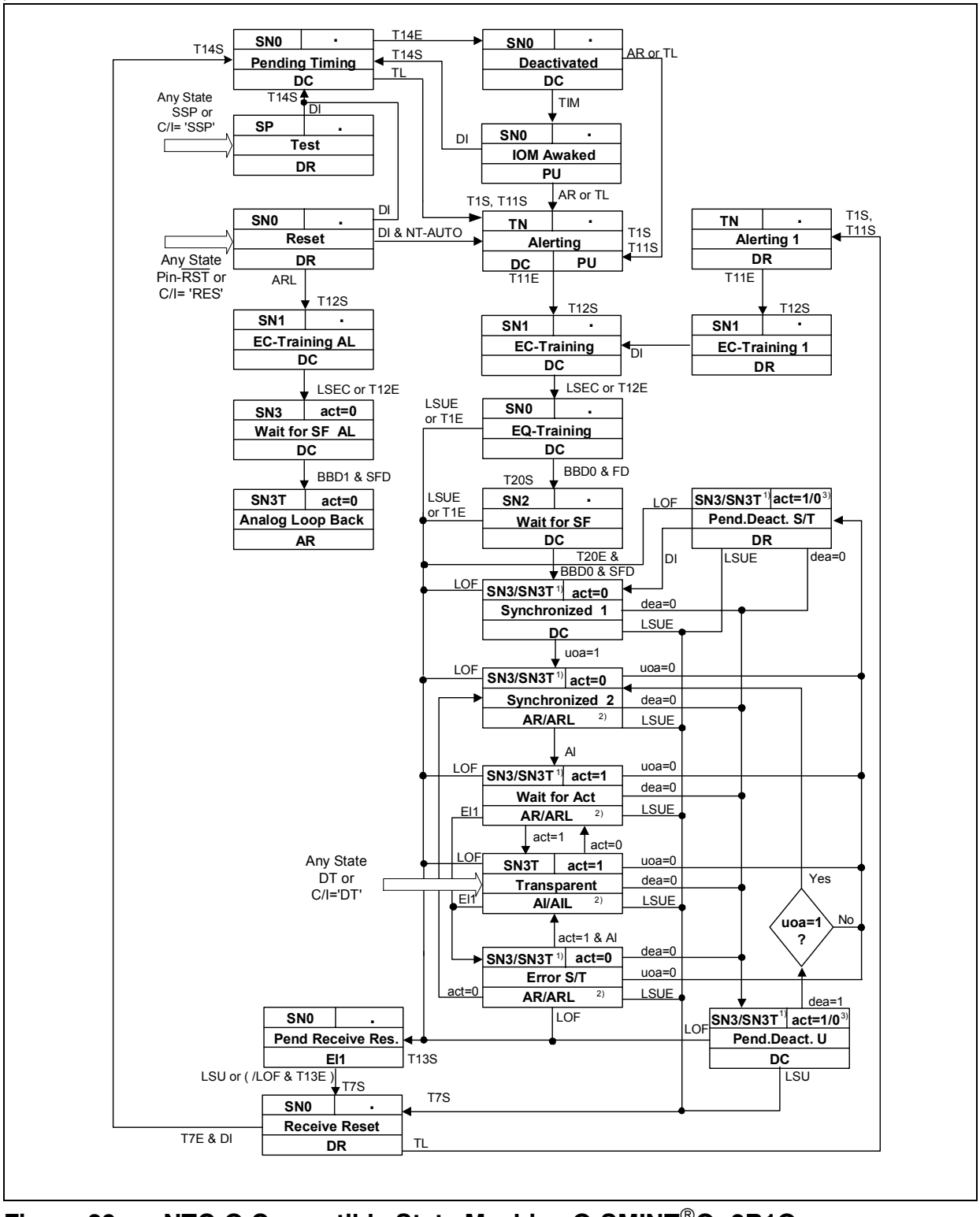


Figure 29 NTC-Q Compatible State Machine Q-SMINT®O: 2B1Q

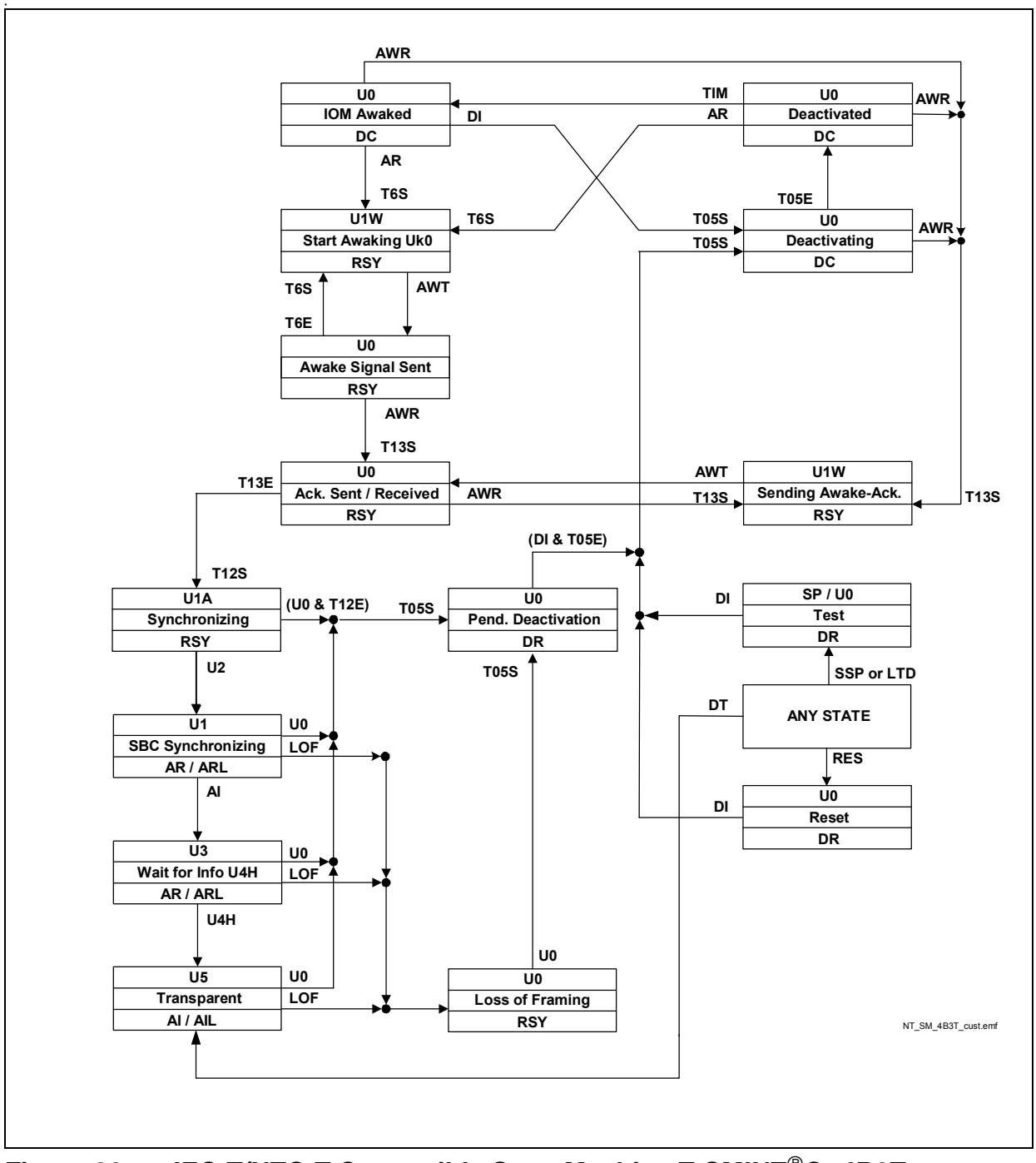


Figure 30 IEC-T/NTC-T Compatible State Machine T-SMINT®O: 4B3T

6.2.3 Command/Indication Codes

Table 32 C/I Codes

Code	Q-SMINT®O: 2B1Q		T-SMINT®O: 4B3T	
	IN	**OUT**	**IN**	**OUT**
0000	TIM	DR	TIM	DR
0001	RES	–	–	–
0010	–	–	–	–
0011	–	–	LTD	–
0100	EI1	EI1	–	RSY
0101	SSP	–	SSP	–
0110	DT	–	DT	–
0111	–	PU	–	–
1000	AR	AR	AR	AR
1001	–	–	–	–
1010	ARL	ARL	–	ARL
1011	–	–	–	–
1100	AI	AI	AI	AI
1101	–	–	RES	–
1110	–	AIL	–	AIL
1111	DI	DC	DI	DC

6.3 External Circuitry

The external circuitry of the Q- and T-SMINT®O is equivalent; however, some external components of the U-transceiver hybrid must be dimensioned different for 2B1Q and 4B3T. All information on the external circuitry is preliminary and may be changed in future documents.

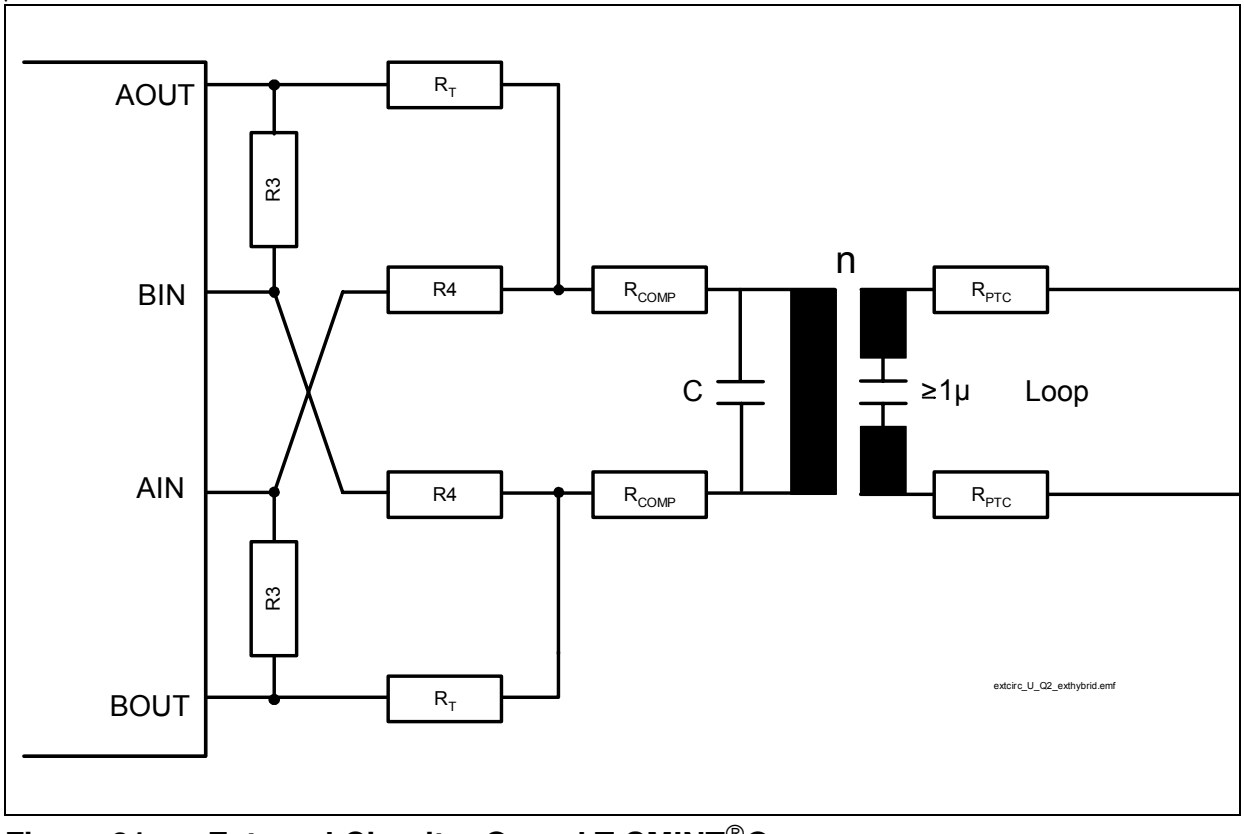


Figure 31 External Circuitry Q- and T-SMINT®O

Note: the necessary protection circuitry is not displayed in **Figure 31**.

Table 33 Dimensions of External Components

Component	Q-SMINT®O: 2B1Q	T-SMINT®O: 4B3T
Transformer: Ratio Main Inductivity	 1:2 14.5 mH	 1:1.6 7.5 mH
Resistance	1.3 kΩ	1.75 kΩ
Resistance	1.0 kΩ	1.0 kΩ
Resistance	9.5 Ω	25 Ω
Capacitor C	27 nF	15 nF
R_{PTC} and R_{Comp}	$2R_{PTC} + 8R_{Comp} = 40\ \Omega$	$n^2 \times (2R_{COMP} + R_B) + R_L = 20\Omega$

7 Index

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