CEL California Eastern Laboratories

Evaluation Board Document

µPC8233TK-EV09-A

Evaluation Board

- Circuit Description
- Typical performance data
- Power gain and isolation plots
- Input and output return loss plots
- Circuit schematic and assembly drawing

Circuit Description

The circuit schematic and assembly drawing are shown on the last two pages.

Matching Circuits

The output matching is mainly through L3 and it should be placed close to the device.

The input matching consists of L1 and C2, and C1 is used for DC block For applications where noise figure is critically important, a high Q inductor, such as wire-wound type, is recommended over regular chip inductor for L1. Using high Q inductors can improve the noise figure by about 0.05dB. The values of L1 and C2 used on this evaluation circuit are chosen for a reasonable balance between input return loss and noise figure. A further trade-off can be made between these two parameters by adjusting the values of L1 and/or C2.

PCB Material

The PCB is FR4 four layer board. The top and bottom dielectric layers are 8mil thick. The total board thickness is 62mil.

Typical Performance Data

Test Conditions:

f=915MHz; Vcc=Vps=1.8V

Noise Figure: 1.3dB (direct measurement on board, no subtraction of board loss)

Gain: 24dB

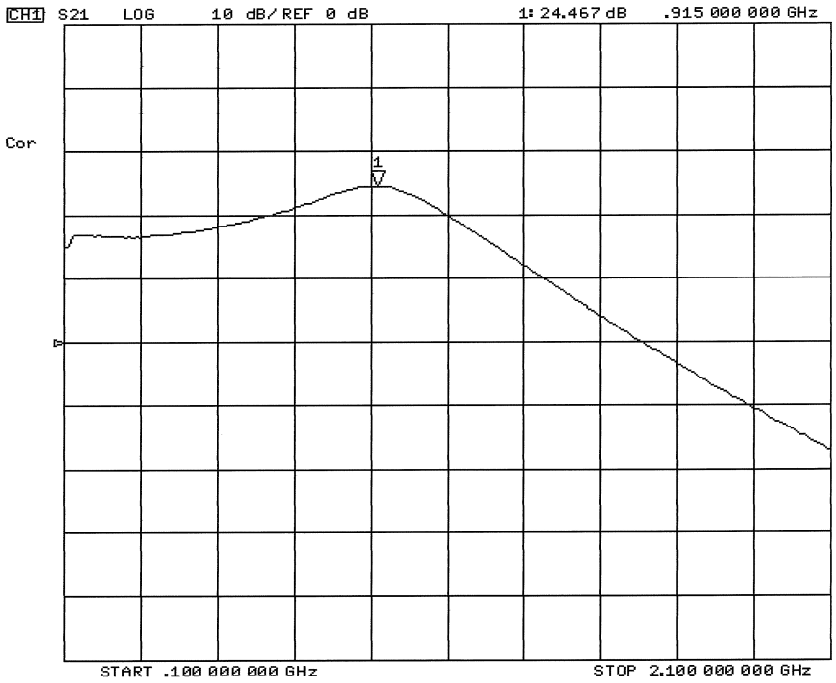
Input return loss: -12dB

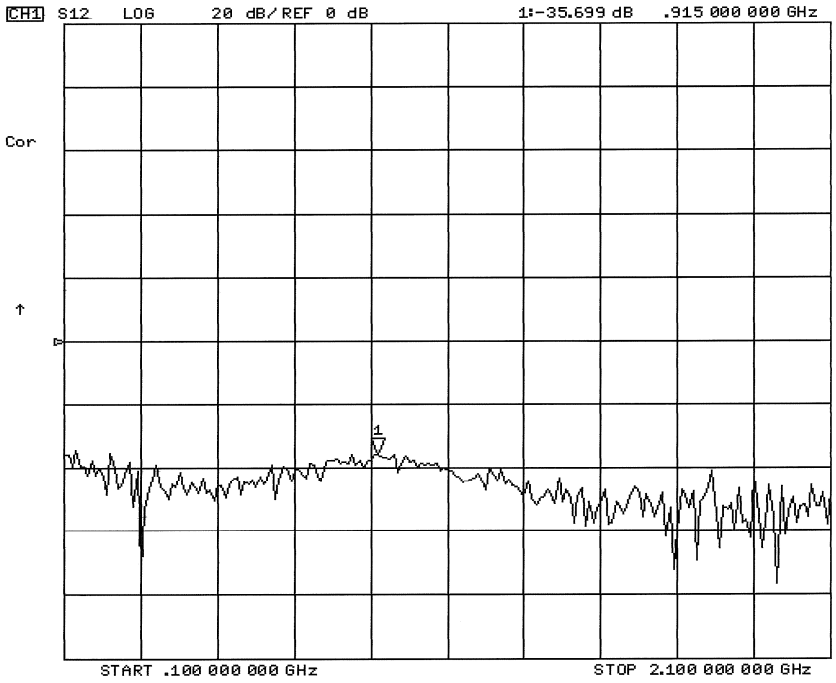
Output return loss: -13dB

IP1dB: -29dBm

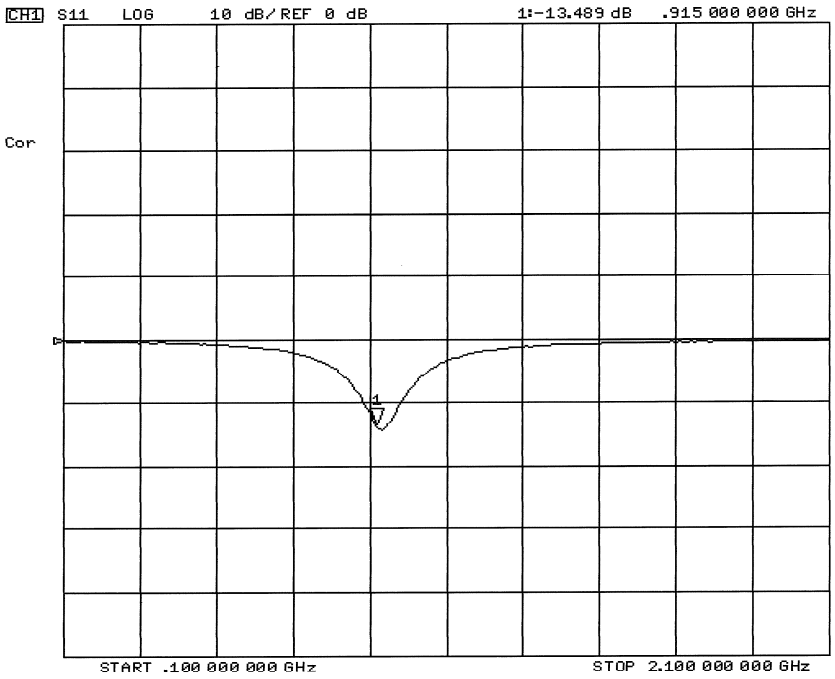
IIP3: -20dBm

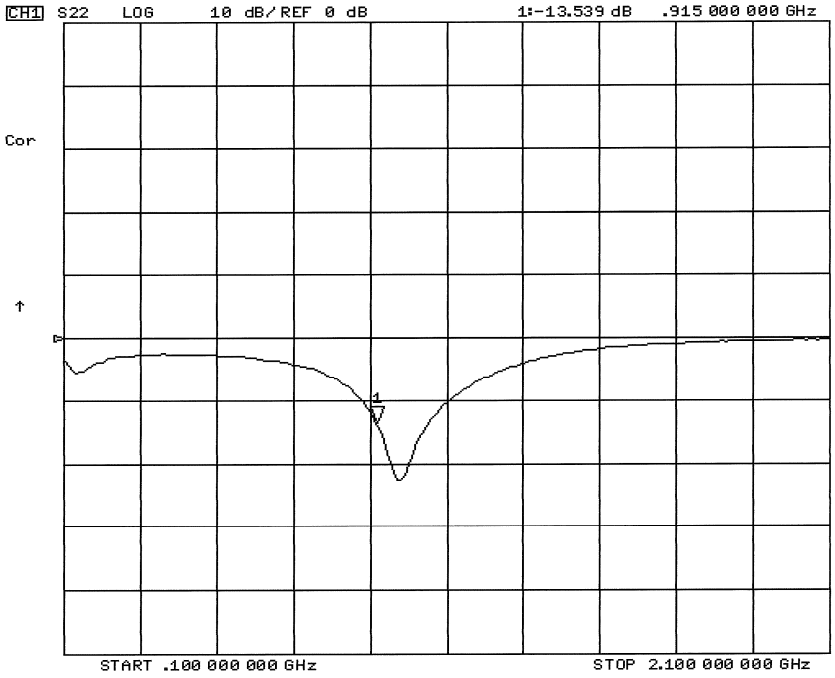
Power Gain and Isolation Plots



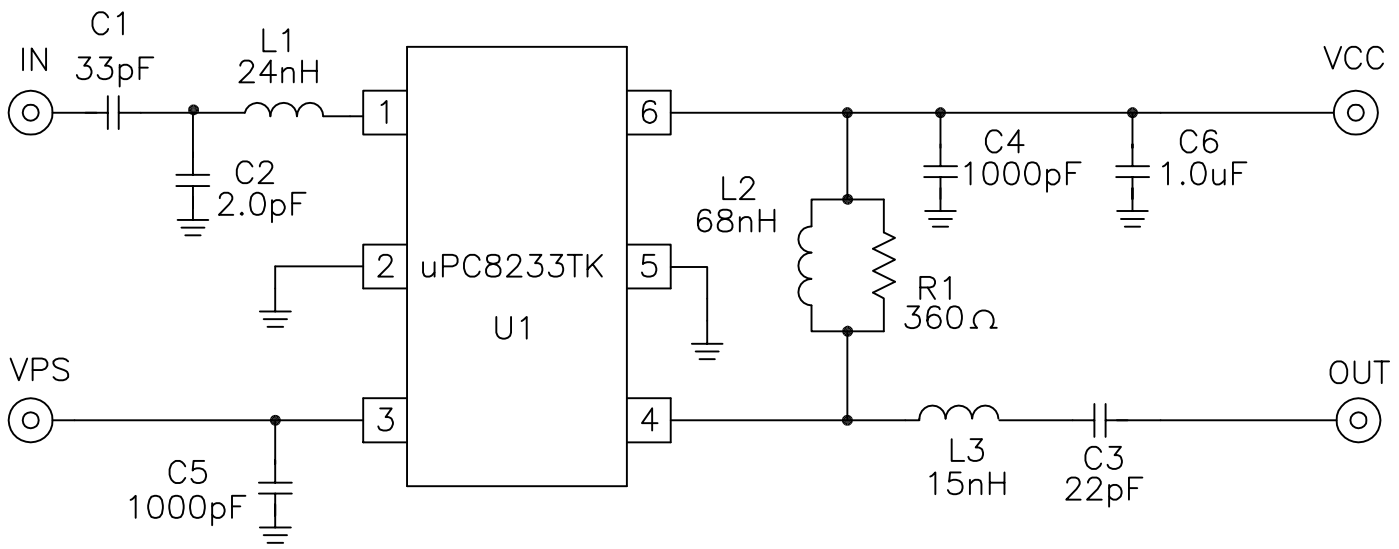


Input and Output Return Loss Plots





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	LQG15HS15NJ02	L3	0402 15nH IND MURATA	13
1	LQG15HS68NJ02	L2	0402 68nH IND MURATA	12
1	LQW15AN24NG00	L1	0402 24nH IND MURATA WIREWOUND	11
1	RK73B1ETTP361J	R1	0402 360 OHMS RES KOA	10
1	GRM155R60J105KE19D	C6	0402 1.0uF CAP MURATA	9
2	GRM1555C1H102JA01D	C4,C5	0402 1000pF CAP MURATA	8
1	GRM1555C1H220JZ01D	C3	0402 22pF CAP MURATA	7
1	GRM1555C1H2R0CZ01D	C2	0402 2.0pF CAP MURATA	6
1	GRM1555C1H330JZ01D	C1	0402 33pF CAP MURATA	5
1	UPC8233TK	U1	IC NEC	4
3	2340-6111 TG	P1,P2,P3	PIN HEADER 3M	3
2	142-0711-821	J1,J2	SMA FEM. E.F. JOHNSON	2
1	CL-101738	DRAWING	COMPONENT LAYOUT DRAWING	1

PARTS LIST

APPROVALS		
Drawing by:	BMU	04/16/2008
Designed by:	BMU	04/16/2008
Checked by:		
Project Engineer:		
Quality Control:		

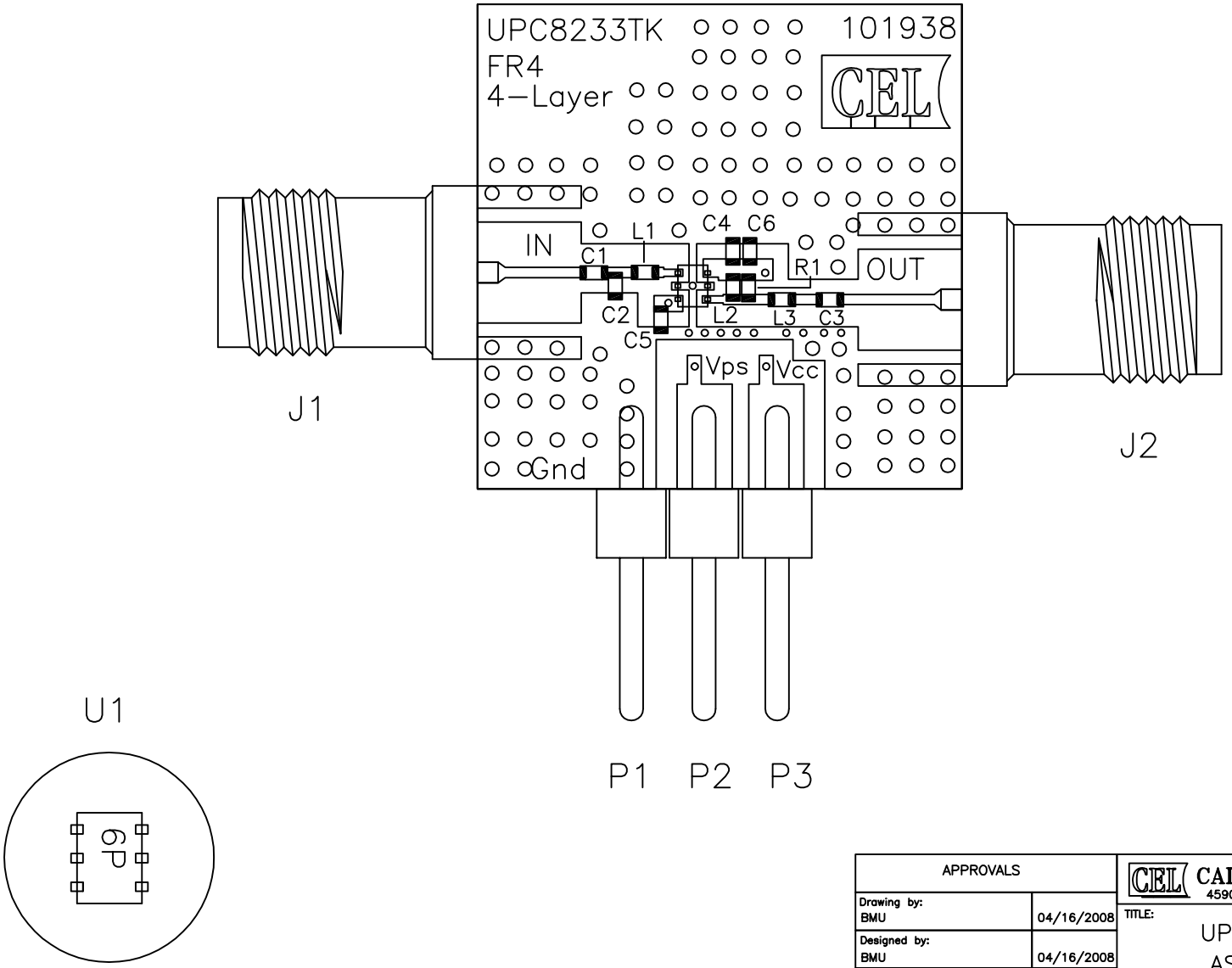
CEL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
UPC8233TK-EV09-A
SCHEMATIC_BOM

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101973	

SCALE SCALE | RELEASE DATE RELDATE | SHEET SHNO OF NOSH

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



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TITLE:
UPC8233TK-EV09-A
ASSEMBLY_DRAWING

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101973	-

SCALE SCALE RELEASE DATE RELDATE SHEET SHNO OF NOSH