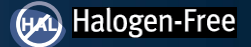


EPC2100 – Enhancement-Mode GaN Power Transistor Half-Bridge

V_{DS} , 30 V

$R_{DS(on)}$, 8.2 mΩ (Q1), 2.1 mΩ (Q2)

I_D , 10 A (Q1), 40 A (Q2)

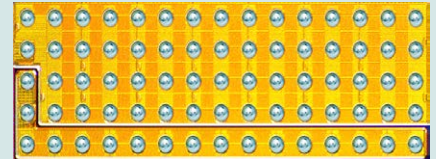


Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

| Maximum Ratings | | | | |
|-----------------|---------------------|--|------------|------|
| DEVICE | PARAMETER | | VALUE | UNIT |
| Q1 | V_{DS} | Drain-to-Source Voltage (Continuous) | 30 | V |
| | | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C) | 36 | |
| | I_D | Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 92^\circ\text{C/W}$) | 10 | A |
| | | Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$) | 100 | |
| | V_{GS} | Gate-to-Source Voltage | 6 | V |
| | | Gate-to-Source Voltage | -4 | |
| | T_J | Operating Temperature | -40 to 150 | °C |
| T_{STG} | Storage Temperature | -40 to 150 | | |
| Q2 | V_{DS} | Drain-to-Source Voltage (Continuous) | 30 | V |
| | | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C) | 36 | |
| | I_D | Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 22^\circ\text{C/W}$) | 40 | A |
| | | Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$) | 400 | |
| | V_{GS} | Gate-to-Source Voltage | 6 | V |
| | | Gate-to-Source Voltage | -4 | |
| | T_J | Operating Temperature | -40 to 150 | °C |
| T_{STG} | Storage Temperature | -40 to 150 | | |

| Thermal Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | |
|---|--|-----|------|
| PARAMETER | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.4 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board | 2.5 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 42 | |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details



EPC2100 eGaN® ICs are supplied only in passivated die form with solder bumps
Die Size: 6.05 mm x 2.3 mm

Applications

- High Frequency DC-DC
- Point-of-Load (POL) Converters

Benefits

- High Frequency Operation
- Ultra High Efficiency
- High Density Footprint

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| DEVICE | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------|--------------|--------------------------------|---|-----|-------|-----|------------|
| Q1 | BV_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0\text{ V}, I_D = 0.3\text{ mA}$ | 30 | | | V |
| | I_{DSS} | Drain-Source Leakage | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ | | 0.004 | 0.2 | mA |
| | I_{GSS} | Gate-to-Source Forward Leakage | $V_{GS} = 5\text{ V}$ | | 0.007 | 3 | mA |
| | | Gate-to-Source Reverse Leakage | $V_{GS} = -4\text{ V}$ | | 0.004 | 0.2 | mA |
| | $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 4\text{ mA}$ | 0.8 | 1.3 | 2.5 | V |
| | $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS} = 5\text{ V}, I_D = 25\text{ A}$ | | 6 | 8.2 | m Ω |
| | V_{SD} | Source-Drain Forward Voltage | $I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$ | | 1.8 | | V |
| Q2 | BV_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$ | 30 | | | V |
| | I_{DSS} | Drain-Source Leakage | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ | | 0.015 | 0.8 | mA |
| | I_{GSS} | Gate-to-Source Forward Leakage | $V_{GS} = 5\text{ V}$ | | 0.03 | 9 | mA |
| | | Gate-to-Source Reverse Leakage | $V_{GS} = -4\text{ V}$ | | 0.015 | 0.8 | mA |
| | $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 16\text{ mA}$ | 0.8 | 1.3 | 2.5 | V |
| | $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS} = 5\text{ V}, I_D = 25\text{ A}$ | | 1.5 | 2.1 | m Ω |
| | V_{SD} | Source-Drain Forward Voltage | $I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$ | | 1.7 | | V |

Dynamic Characteristics

| DEVICE | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------|---------------|---|--|-----|------|------|------|
| Q1 | C_{ISS} | Input Capacitance | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$ | | 395 | 475 | pF |
| | C_{RSS} | Reverse Transfer Capacitance | | | 15 | | |
| | C_{OSS} | Output Capacitance | | | 290 | 435 | |
| | $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{DS} = 0\text{ to }15\text{ V}, V_{GS} = 0\text{ V}$ | | 371 | | |
| | $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3) | | | 404 | | |
| | Q_G | Total Gate Charge | $V_{DS} = 15\text{ V}, V_{GS} = 5\text{ V}, I_D = 25\text{ A}$ | | 3.6 | 4.9 | nC |
| | Q_{GS} | Gate-to-Source Charge | $V_{DS} = 15\text{ V}, I_D = 25\text{ A}$ | | 1.3 | | |
| | Q_{GD} | Gate-to-Drain Charge | | | 0.6 | | |
| | $Q_{G(TH)}$ | Gate Charge at Threshold | | | 0.9 | | |
| | Q_{OSS} | Output Charge | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$ | | 6.1 | 9.2 | |
| | Q_{RR} | Source-Drain Recovery Charge | | | 0 | | |
| Q2 | C_{ISS} | Input Capacitance | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$ | | 1630 | 1960 | pF |
| | C_{RSS} | Reverse Transfer Capacitance | | | 64 | | |
| | C_{OSS} | Output Capacitance | | | 1370 | 2060 | |
| | $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{DS} = 0\text{ to }15\text{ V}, V_{GS} = 0\text{ V}$ | | 1740 | | |
| | $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3) | | | 1900 | | |
| | Q_G | Total Gate Charge | $V_{DS} = 15\text{ V}, V_{GS} = 5\text{ V}, I_D = 25\text{ A}$ | | 15 | 19 | nC |
| | Q_{GS} | Gate-to-Source Charge | $V_{DS} = 15\text{ V}, I_D = 25\text{ A}$ | | 4.8 | | |
| | Q_{GD} | Gate-to-Drain Charge | | | 2.7 | | |
| | $Q_{G(TH)}$ | Gate Charge at Threshold | | | 3.4 | | |
| | Q_{OSS} | Output Charge | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$ | | 29 | 44 | |
| | Q_{RR} | Source-Drain Recovery Charge | | | 0 | | |

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1a (Q1): Typical Output Characteristics at 25°C

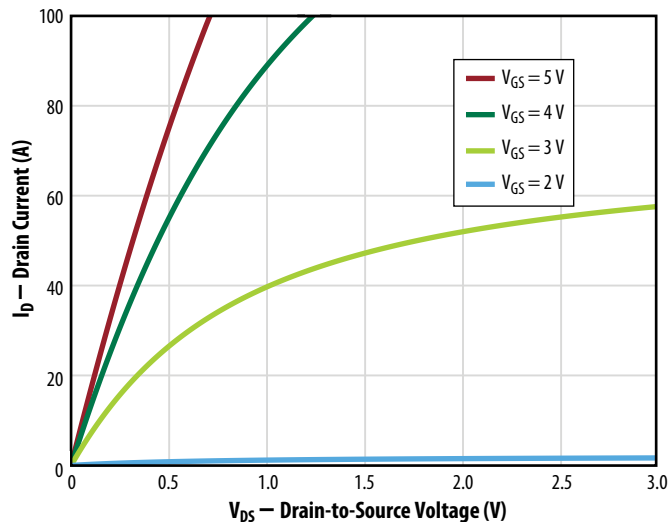


Figure 1b (Q2): Typical Output Characteristics at 25°C

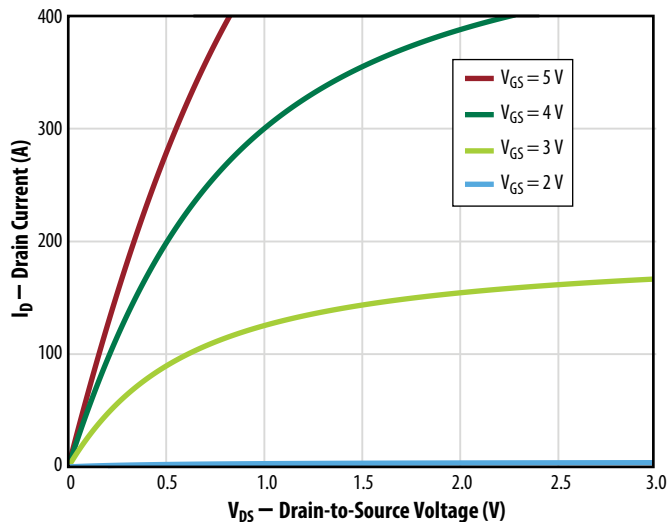


Figure 2a (Q1): Transfer Characteristics

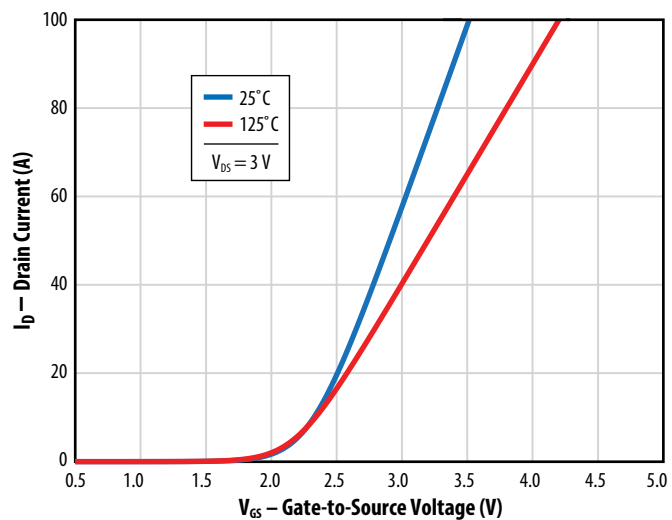


Figure 2b (Q2): Transfer Characteristics

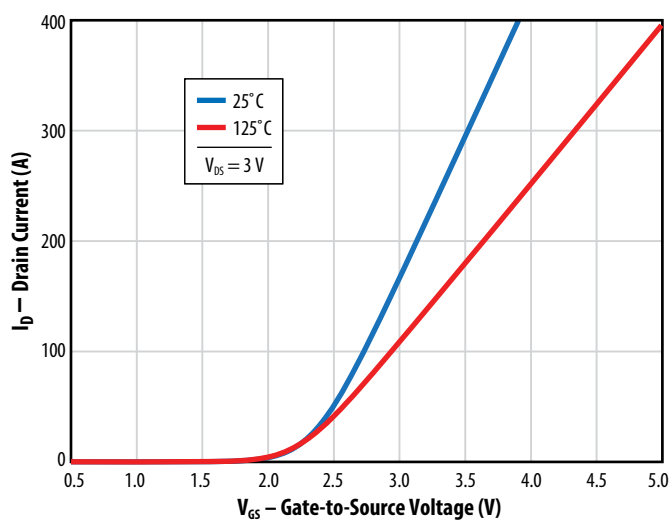


Figure 3a (Q1): $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

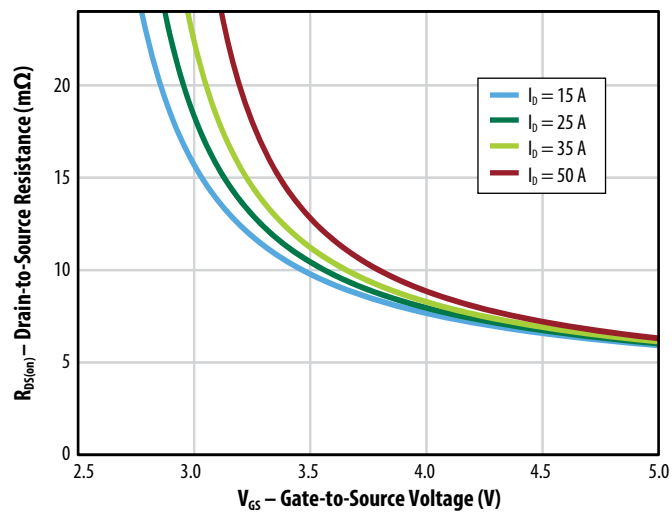


Figure 3b (Q2): $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

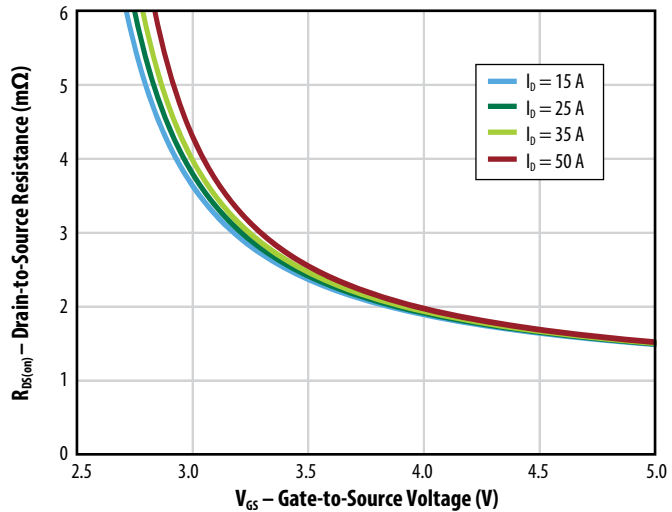


Figure 4a (Q1): $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

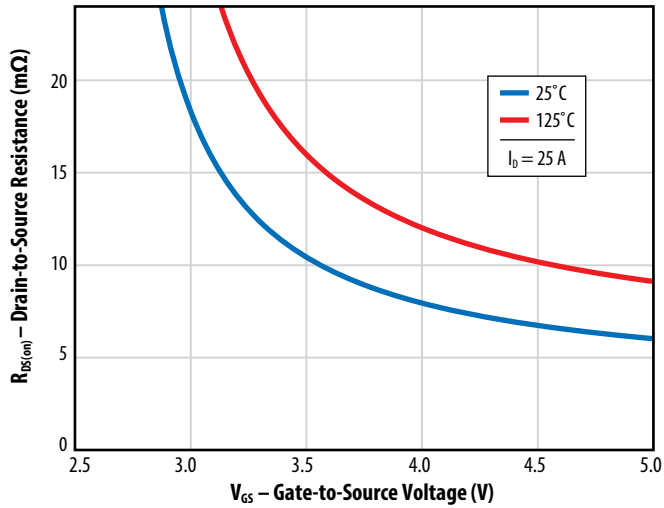


Figure 4b (Q2): $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

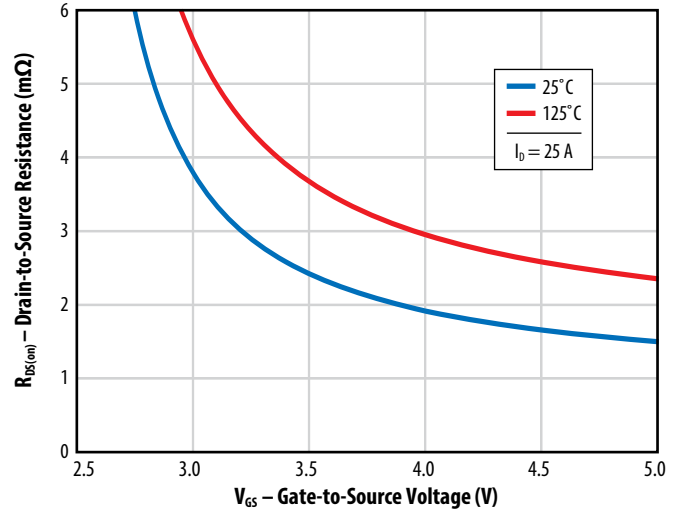


Figure 5a (Q1): Capacitance (Linear Scale)

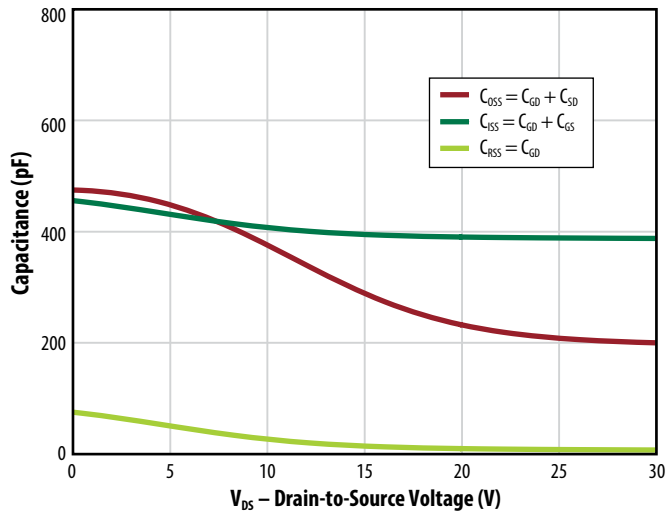


Figure 5b (Q1): Capacitance (Log Scale)

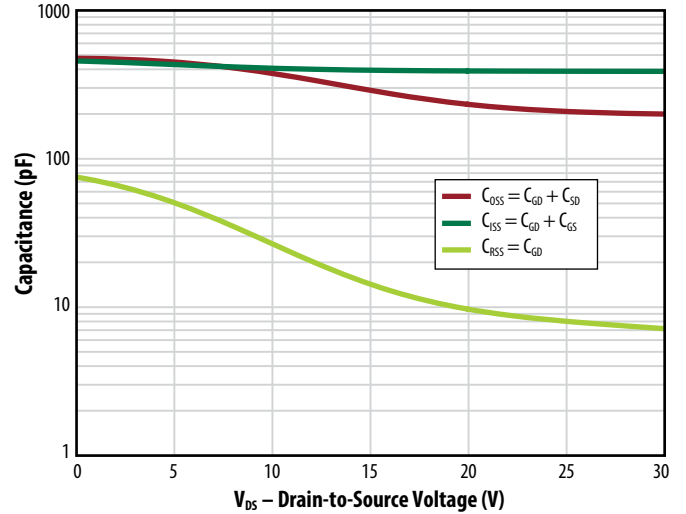


Figure 5c (Q2): Capacitance (Linear Scale)

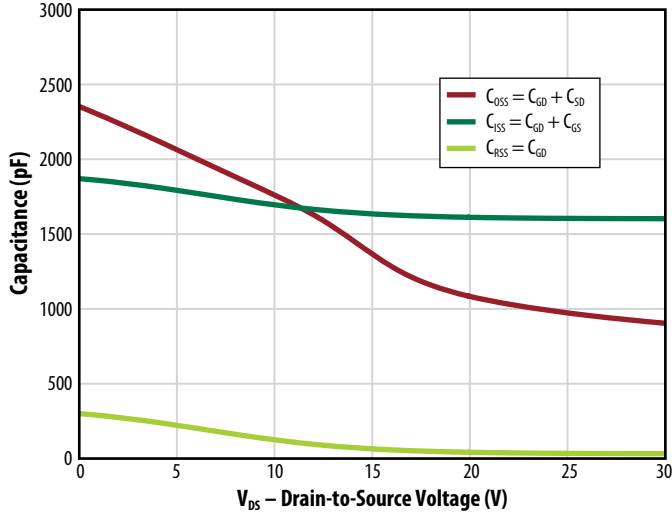


Figure 5d (Q2): Capacitance (Log Scale)

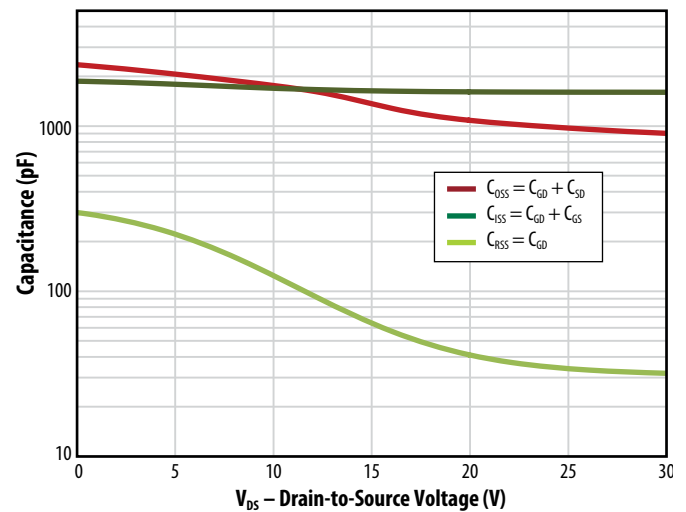


Figure 6a (Q1): Output Charge and C_{OSS} Stored Energy

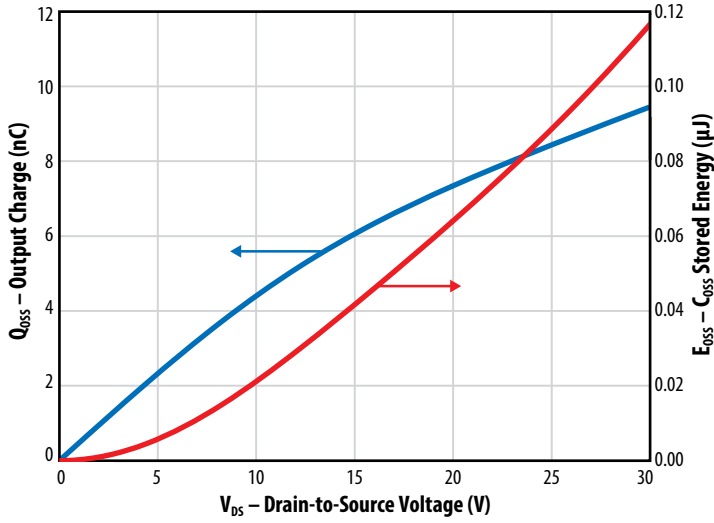


Figure 6b (Q2): Output Charge and C_{OSS} Stored Energy

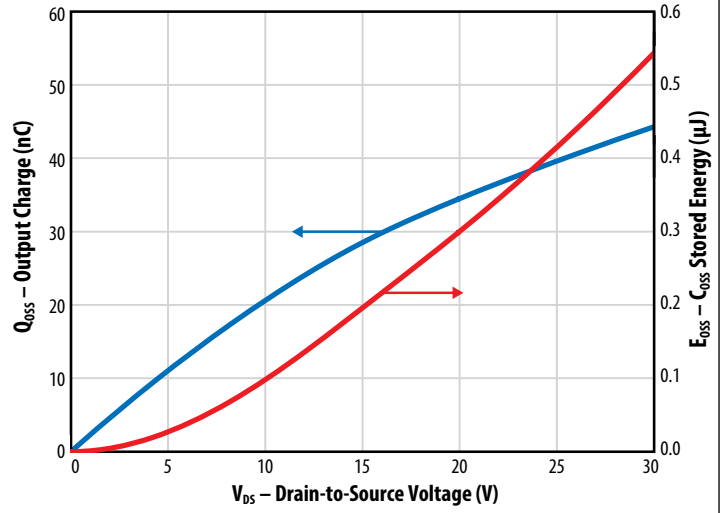


Figure 7a (Q1): Gate Charge

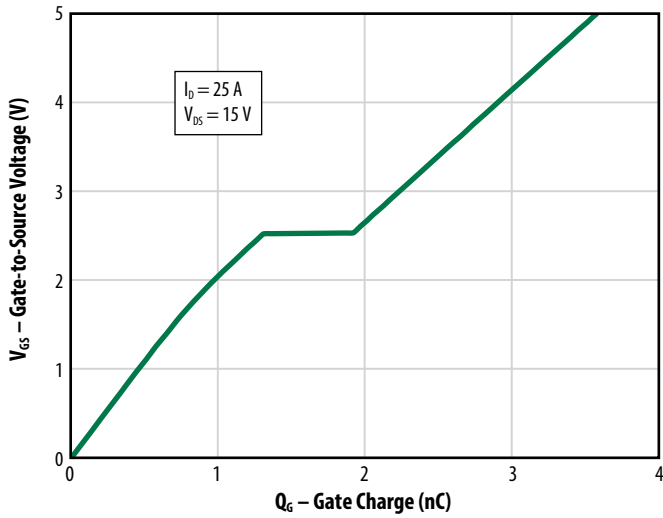


Figure 7b (Q2): Gate Charge

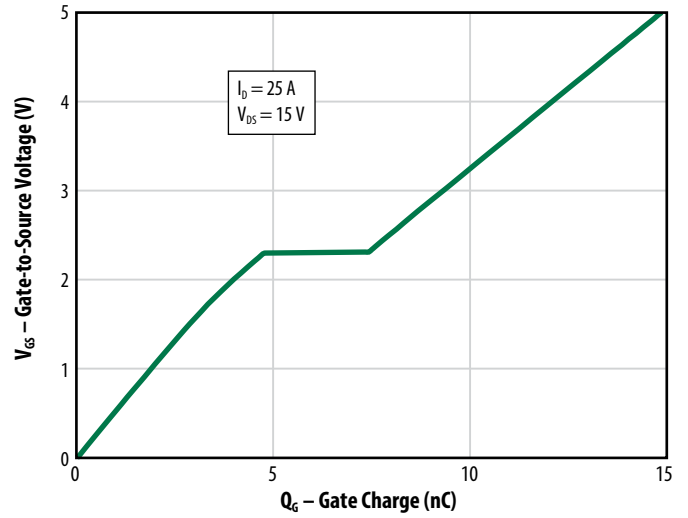


Figure 8a (Q1): Reverse Drain-Source Characteristics

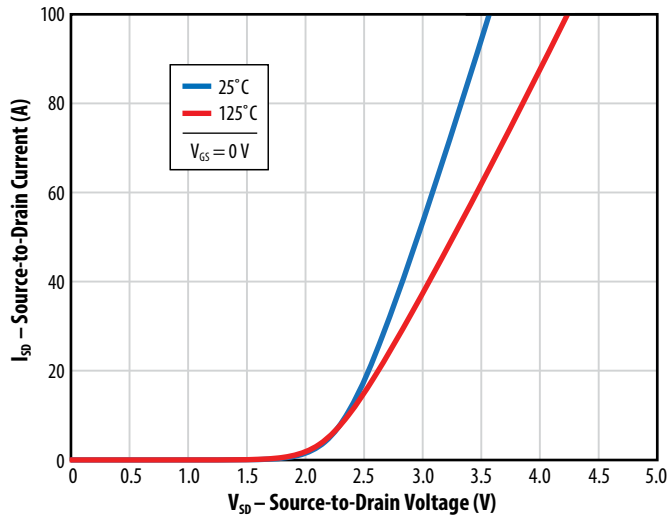


Figure 8b (Q2): Reverse Drain-Source Characteristics

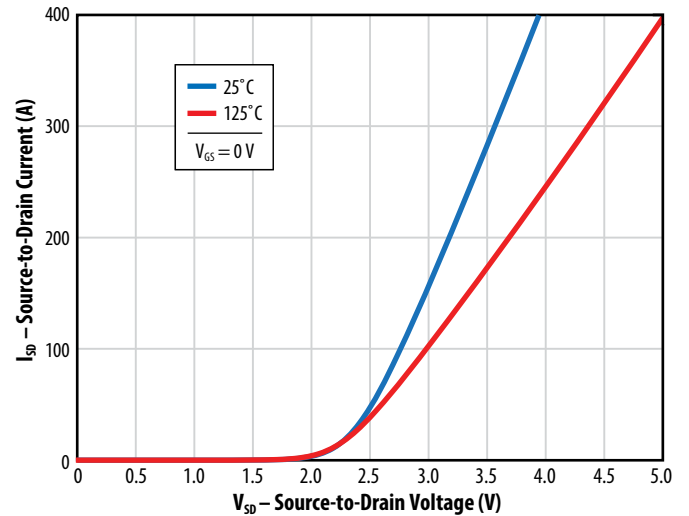


Figure 9a (Q1):
Normalized On-State Resistance vs. Temperature

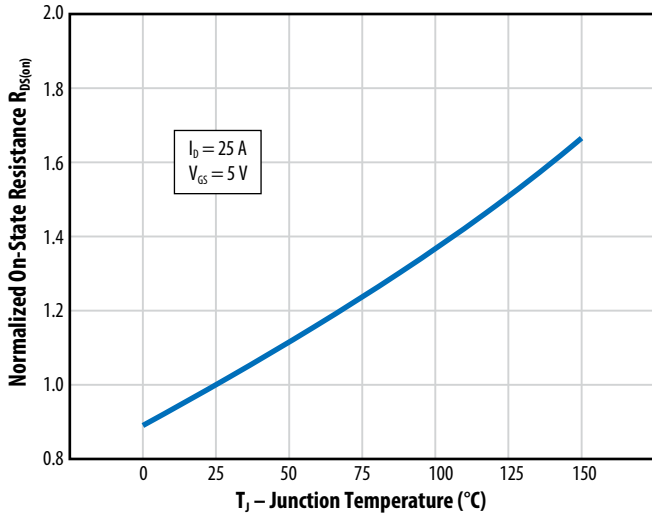


Figure 9b (Q2):
Normalized On-State Resistance vs. Temperature

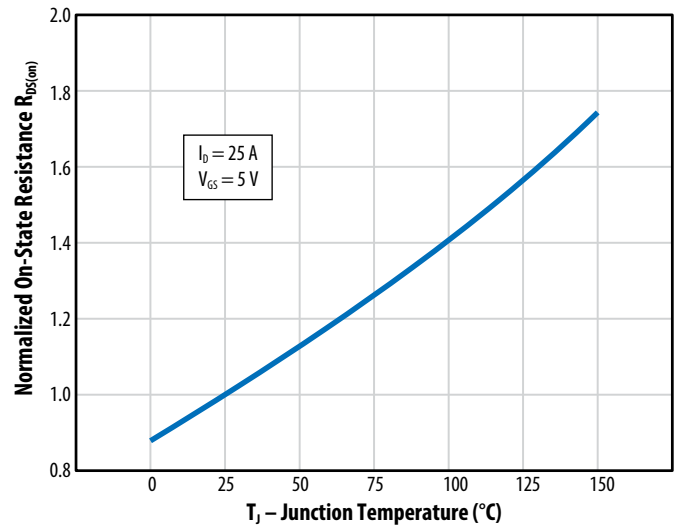


Figure 10a (Q1):
Normalized Threshold Voltage vs. Temperature

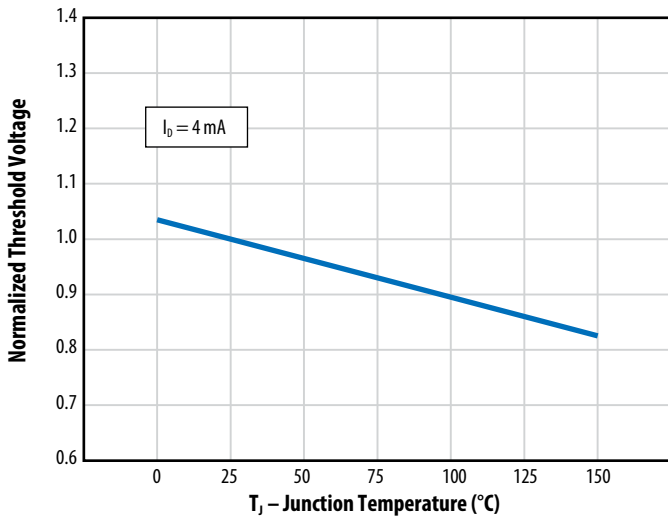


Figure 10b (Q2):
Normalized Threshold Voltage vs. Temperature

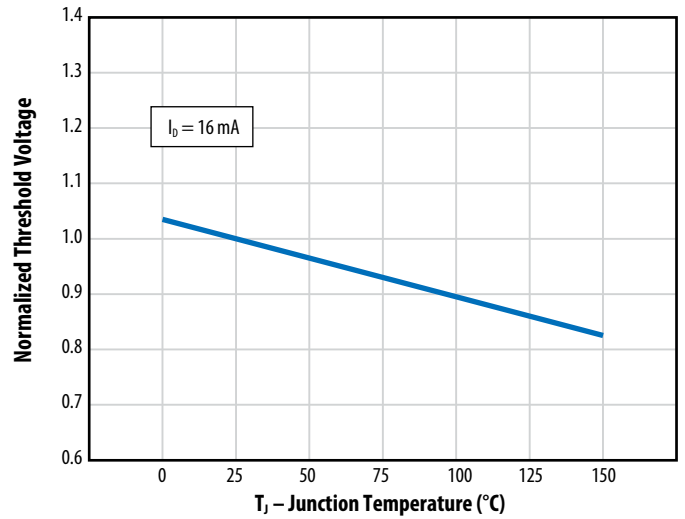


Figure 11a (Q1): Safe Operating Area

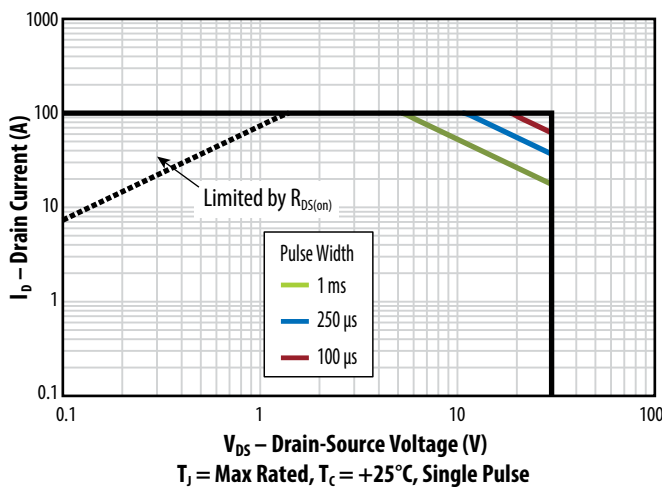


Figure 11b (Q2): Safe Operating Area

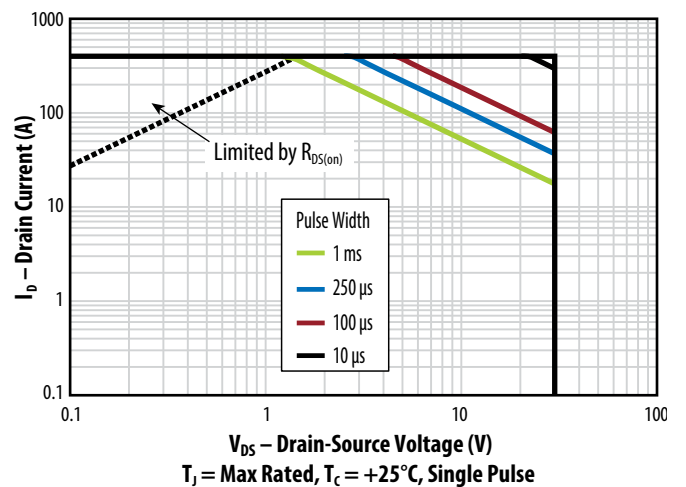


Figure 12a
Transient Thermal Response Curves

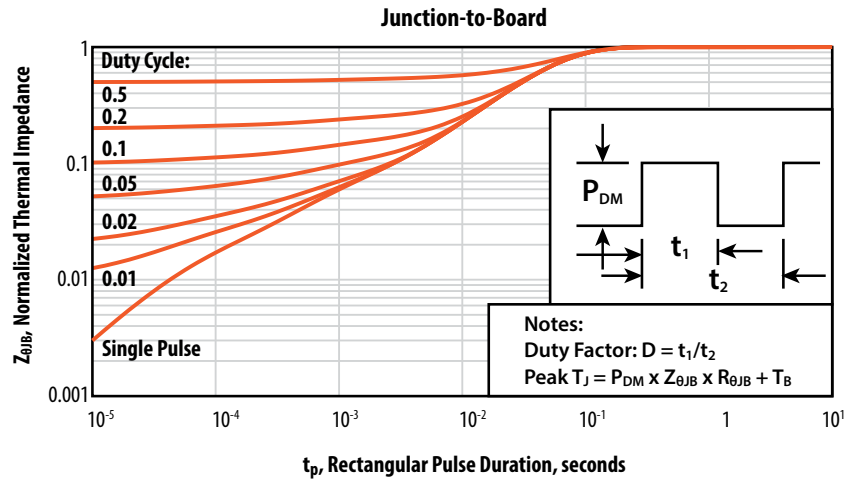


Figure 12b
Transient Thermal Response Curves

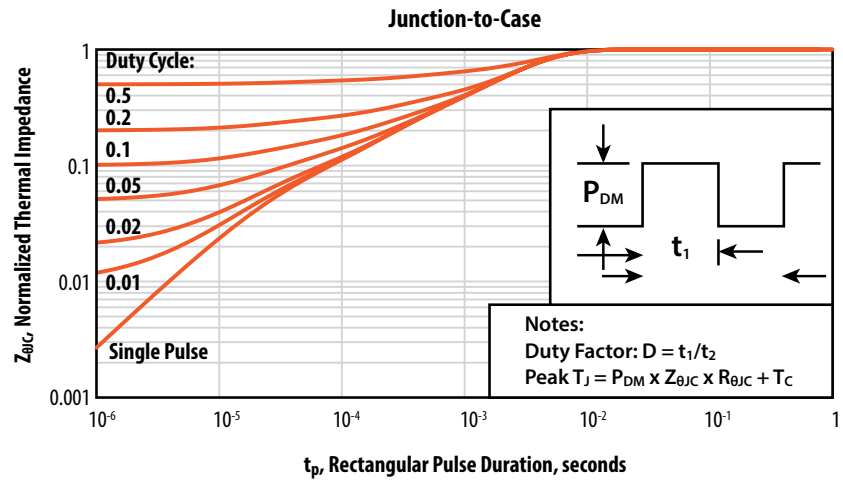
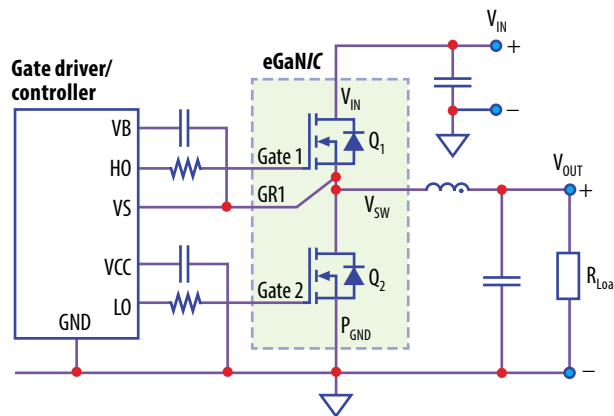
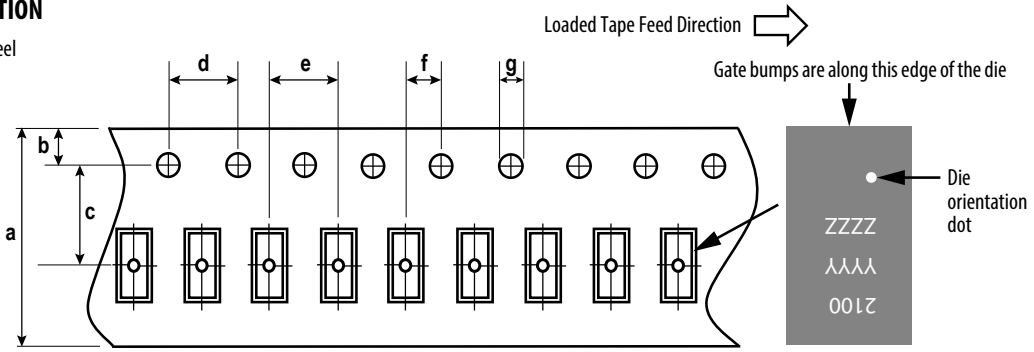
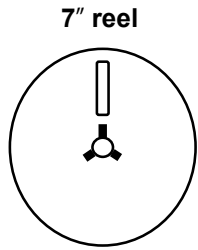


Figure 13
Typical Application Circuit



TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel

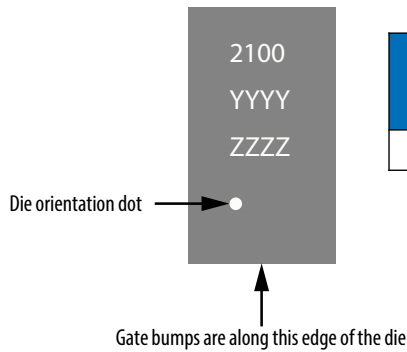


Die is placed into pocket solder ball side down (face side down)

| EPC2100 (note 1) | | | |
|------------------|--------|-------|-------|
| Dimension (mm) | target | min | max |
| a | 12.00 | 11.70 | 12.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (see note) | 5.50 | 5.45 | 5.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (see note) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.50 | 1.60 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

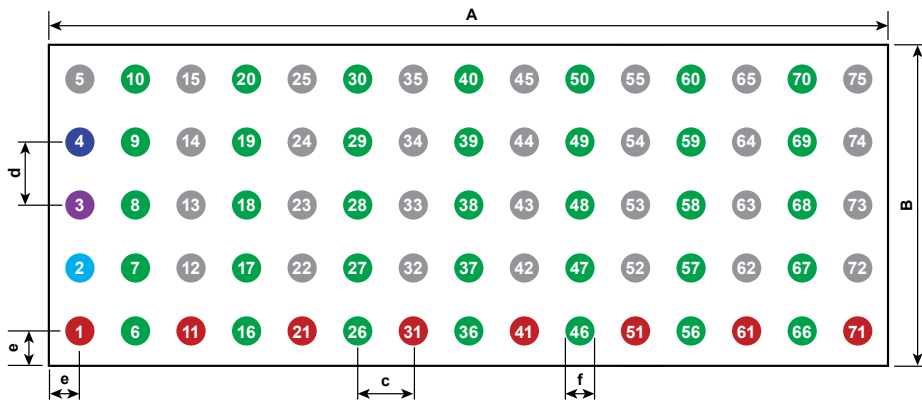
DIE MARKINGS



| Part Number | Laser Markings | | |
|-------------|-----------------------|------------------------------|------------------------------|
| | Part # Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
| EPC2100 | 2100 | YYYY | ZZZZ |

DIE OUTLINE

Solder Bump View



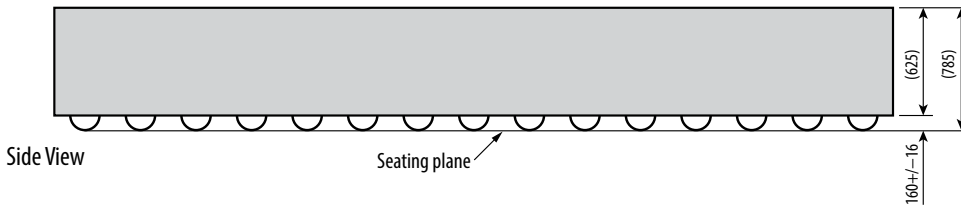
| DIM | MIN | Nominal | MAX |
|-----|------|---------|------|
| A | 6020 | 6050 | 6080 |
| B | 2270 | 2300 | 2330 |
| c | 400 | 400 | 400 |
| d | 450 | 450 | 450 |
| e | 210 | 225 | 240 |
| f | 187 | 208 | 240 |

Pad 2 is Gate1 (high side); Pad 4 is Gate2 (low side); Pad 3 is HS Gate Return;

Pads 5, 12, 13, 14, 15, 22, 23, 24, 25, 32, 33, 34, 35, 42, 43, 44, 45, 52, 53, 54, 55, 62, 63, 64, 65, 72, 73, 74, 75 are Ground;

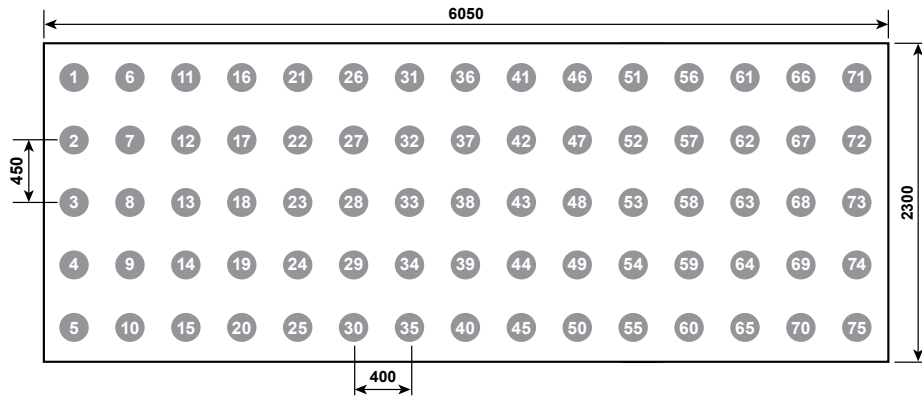
Pads 1, 11, 21, 31, 41, 51, 61, 71 are V_{IN} ;

Pads 6, 7, 8, 9, 10, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are Switch Node



RECOMMENDED LAND PATTERN

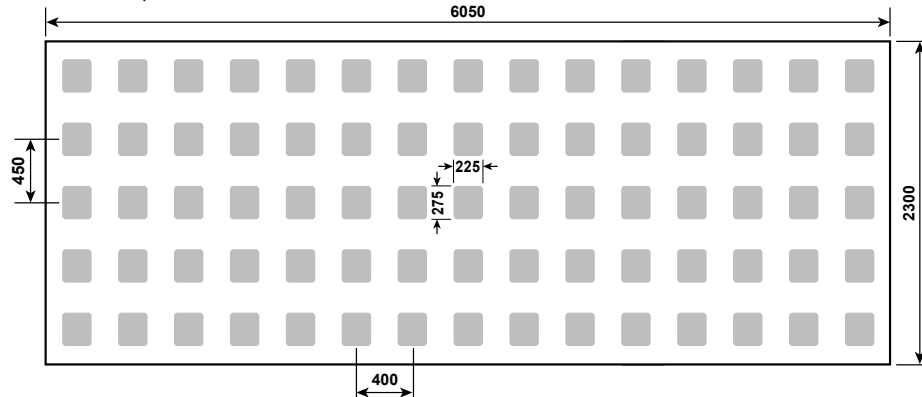
(measurements in μm)



The land pattern is solder mask defined. Suggest SMD Pads at $200 +20/-10 \mu\text{m}$. $190 \mu\text{m}$ minimum.

RECOMMENDED STENCIL DRAWING

(measurements in μm)



Recommended stencil should be 4 mil ($100 \mu\text{m}$) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at: <https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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EPC Patent Listing: epc-co.com/epc/AboutEPC/Patents.aspx

Information subject to change without notice.

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